ON-LINE DIGITAL CORRECTION OF THE HARMONIC DISTORTION IN ANALOG-TO-DIGITAL CONVERTERS

U. Eduri
kiran@ee.tamu.edu

F. Maloberti
franco@ee.tamu.edu

Department of Electrical Engineering, Texas A&M University, College Station, TX 77843, USA

ABSTRACT

A digital calibration technique for the on-line (real-time) correction of the Integral Nonlinearity (INL) in any Analog-to-Digital Converter (ADC) has been presented in this paper. MATLAB simulations substantiating the technique achieved around 20 dB improvement on a modeled 12-bit ADC with an initial Spurious-Free Dynamic Range of 80 dBFS. As a bonus, this technique can also correct for the offset error. The price paid for these benefits is the inclusion of an identical extra ADC, and some additional DSP circuitry.

1. INTRODUCTION AND BACKGROUND

Ever-increasing demand on the performance-requirements of the ADCs, particularly in the area of wireless communications, where it is highly desirable to have the data converter as close to the antenna as possible, has forced very tight requirements on both speed and accuracy of data conversion. While sampling frequency is a measure of the speed, accuracy is measured in terms of the Signal-to-Noise Ratio (SNR) and Spurious-Free Dynamic Range (SFDR), in addition to the number of bits for resolution. Because of the intrinsic high sensitivity of harmonic distortion to even small non-idealities in sampled-data systems, achieving a high value of SFDR (> 90 dB for a 12-bit 65 MSps ADC) has been very difficult and expensive, particularly on the analog side of the data converter. Even a very good initial calibration would fail to account for the aging effects that degrade the performance of an ADC.

Several methods to compensate for ADC nonlinearity have been proposed in the digital domain. The methods proposed in [1], [2], [3] and [4] are specific for the ADC targeted. The method proposed in [5] is more general but specific for those ADCs based on successive approximation.

Methods for off-line correction of nonlinearity have been proposed in [6], [7] and [8]. However, these proposals cannot correct for the aging effects. An on-line correction technique has been proposed in [8], but it requires the use of a master ADC with higher resolution but lower speed than the slave (field) converter. In this paper, an alternate scheme, wherein two nominally identical ADCs are used in the master-slave configuration, is proposed. The distorted output of the ADC is passed through a correction block whose parameters are updated at regular intervals by means of a mechanism that continuously monitors and estimates the nonlinearity in the converter.

2. BASIC IDEA OF THE TECHNIQUE

Fig.1 shows the schematic implementation of the proposed technique at the system level. There are two identical ADCs, which are perfectly matched (which will be extended to mismatched ADCs later in this paper), one taking the on-line input and the other taking an attenuated version of the same. Based on the mapping between the observed output sequences, $\{y_1\}$ and $\{y_2\}$, for a set of unknown inputs $\{x\}$ spread over the entire dynamic range, the nonlinearity in these ADCs can be estimated and corrected for.

Let us start with an ADC of infinite resolution, that is, with no quantization error but only nonlinearity. Suppose the output to input relationship of this ADC is given by $y = f(x)$. Then, cascading with it a correction block, whose output to input relationship is $z = f^{-1}(y)$, will imply that $z = x$. We are interested in the f^{-1} , rather than f itself. For this reason, and also for its intrinsic suitability to the proposed technique, the nonlinearity has been modeled in terms of an n th-order polynomial as shown in (1).

$$x = f^{-1}(y) = \sum_{j=0}^n a_j y^j \quad (1)$$

Fig.1 – Schematic representation of the proposed technique

Since only the nonlinearity, but not gain error is of interest in this paper, all coefficients can be normalized with respect to the coefficient of the first-order term. In such a case, without loss of generality, we can set $a_1=1$. Now, looking at Fig.1, we can write, for any given x_i belonging to $\{x\}$ with n elements (for obtaining n independent equations to solve for n variables, $a_0, a_2, a_3, \dots, a_n$),

$$x_i = f^{-1}(y_{1i}) = a_0 + y_{1i} + \sum_{j=2}^n a_j y_{1i}^j \quad (2)$$

$$kx_i = f^{-1}(y_{2i}) = a_0 + y_{2i} + \sum_{j=2}^n a_j y_{2i}^j \quad (3)$$

Eliminating x_i between (2) and (3), and retaining known y_{1i} and y_{2i} ,

$$(1-k)a_0 + \sum_{j=2}^n (y_{2i}^j - ky_{1i}^j)a_j = -(y_{2i} - ky_{1i}) \quad (4)$$

We have a set of n simultaneous linear equations with n variables, $a_0, a_2, a_3, \dots, a_n$, given by (4), which can be solved easily. However, the solution to this problem is not this simple because of the following limitations:

- (i) Quantization error caused by the finite resolution,
- (ii) Mismatch between the two ADCs, and (iii) Uncertainty in the value of k .

These limitations can be overcome by following the remedies given in the subsequent sections.

3. QUANTIZATION ERROR

The ADC is seen as a combination of a nonlinear function (continuous output voltage), which has to be corrected for, and an ideal quantizer

(discrete output voltage). Uniform Probability Distribution Function (PDF) for the quantization error is assumed, as given in Fig.2, where $\Delta = FS/2^b$ is the quantization step-size of a b -bit ADC with full scale, FS . It is also assumed that the nonlinearity is small enough so that it does not alter the nature of randomness. (For example, an input vector with uniformly spread elements within its domain would produce a vector with uniformly spread elements at the output of the nonlinear function.) In order for the quantization not to mask the nonlinearity, an average value of a sufficiently large number of ADC output samples is required, such that the quantization error of these samples follows the uniform PDF of Fig.2, and cancels out through averaging.

Fig.2 – Probability Distribution Function of Quantization error

Let a total of x_{total} input samples (uniformly spread over a range) produce hits on exactly m consecutive output quantization levels. Let x_{min} and x_{max} be the hit-count respectively on the minimum quantization level (v_{min}) and the maximum quantization level (v_{max}) $\exists m=1+(v_{max}-v_{min})/\Delta$. Then it can be shown that the average value of these samples at the input of ideal quantizer (taking into consideration, residual quantization error) is approximately given by,

$$\frac{v_{min} + v_{max}}{2} + \left(\frac{x_{min} - x_{max}}{2x_{total}} \right) [v_{min} - v_{max} + \Delta\lambda] \quad (5)$$

where $\lambda = 1 + \frac{(m-2)(x_{min} + x_{max})}{x_{total} - x_{min} - x_{max}}$

4. MISMATCH BETWEEN THE ADCs AND UNCERTAINTY IN k

Even though care may be taken to minimize the mismatch between the two ADCs (for example,

by following good layout techniques), it is nevertheless present and can seriously degrade the effectiveness of the scheme. Likewise, the effectiveness of the scheme depends significantly on the accuracy of k . In the presence of these two limitations, the data path of ADC2 can be seen, essentially, as a cascade of a perfectly linear attenuator of *unknown* value k , and an ADC2 mismatched with ADC1 only for offset error and nonlinearity. Gain-error mismatch is absorbed into the uncertainty in k . Under mismatch conditions thus modeled, (3) and (4) are modified respectively as,

$$kx_i = (a_0 + \delta a_0) + y_{2i} + \sum_{j=2}^n (a_j + \delta a_j) y_{2i}^j \quad (6)^1$$

$$(1-k)a_0 + \delta a_0 + \sum_{j=2}^n (y_{2i}^j - ky_{1i}^j) a_j + \sum_{j=2}^n y_{2i}^j \delta a_j = -(y_{2i} - ky_{1i}) \forall i = 1, 2, \dots, N \quad (7)$$

where $\delta a_j, j=0, 2, 3, \dots, n$, are the differences between the respective coefficients, $a_0, a_2, \dots, a_n$, of the two ADCs, and $N=2n$. ($N=2n$, because there are $2n$ variables, $k, A_0 \equiv (1-k)a_0 + \delta a_0, a_2, \dots, a_n, \delta a_2, \dots, \delta a_n$; it can be easily shown that a_0 and δa_0 cannot be solved for individually, for a given k .)

It is to be noted that the $\{y_{1i}\}$ and $\{y_{2i}\}$ used here are not single samples but appropriate averages (as described in Section 3) of a number of samples at the outputs of the corresponding ADCs. Moreover, (7) are no longer linear simultaneous equations, but are nonlinear because k is also a variable. It can be shown that the first $(N-1)$ equations can be solved for as linear simultaneous equations in terms of k and substituted for in the N^{th} equation, to give an equation of the form given in (8).

$$k(k - k_r) = 0 \quad (8)$$

Since $k=0$ is clearly an extraneous solution, $k=k_r$. Substituting for k , all the required variables can be evaluated.

5. OFFSET ERROR CORRECTION

¹ It is to be noted that k can be equal to 1, if there is some "perceivable" mismatch!

Fig.3 – Final Implementation for the case that includes Offset Correction

The inability of the scheme to evaluate both a_0 and δa_0 simultaneously, results in a residual offset error even after correction, if a_0 is approximated as $A_0/(1-k)$. If offset error is to be corrected better, the whole sequence should be repeated for a different value of k . However, care should be taken such that the values of a_0 and δa_0 are the same for both k 's. This can be ensured if a simple passive voltage divider is used for attenuation. Then, it can be shown that,

$$a_0 = \frac{A_{01} - A_{02}}{k_2 - k_1} \quad (9)$$

where $A_0 = A_{0i}$, when $k = k_i$. The final implementation is as shown in Fig.3.

6. IMPLEMENTATION TO THE BENCHMARK SITUATION

A 12-bit ADC with an initial level of harmonic distortion of 80 dBFS (dominated by the third harmonic, assuming a fully differential architecture for circuit implementation) and an offset error of -50 dBFS, has been modeled using MATLAB. A 5% mismatch was also modeled. The same software has been used to implement the whole of the nonlinearity-correction scheme. An improvement of about 20 dB in the SFDR and reduction of offset by over 30 dB have been achieved when n has been chosen as 3, and the values for k have been chosen as 1 and 0.5. (It is to be noted that $k=1$ can result in a singularity if there is no sufficient mismatch!) Statistical averaging, to

Fig.4 – (a) Frequency plot of the distorted signal (b) Frequency plot of corrected signal

reduce quantization error, involved collection of 2^{13} samples per 5 quantization levels on ADC2 (more than one quantization level in order to average out the local variations due to Differential Nonlinearities (DNL)), and averaging their corresponding mapped values on ADC1, which is equivalent to about a 10-bit improvement in resolution. All processing has been done using double-precision arithmetic. Fig.4(a) and Fig.4(b) respectively represent the DFT plots of the distorted and corrected signals when the ADC was fed with a pure tone of amplitude covering the entire dynamic range. In the case illustrated, the second harmonic in the corrected signal is significantly higher than the third, and is the one actually determining the SFDR. This unexpected behavior is attributed to the approximations made while modeling, including the finite order of correction coefficients and mismatch modeling. Repeated simulations have, however, achieved an overall SFDR of over 100 dBFS consistently, which is over 20 dB improvement from the starting value.

7. CONCLUSION

An on-line digital correction technique to improve the linearity of any ADC has been proposed. MATLAB simulations showed an improvement of about 20 dB over the initial SFDR level of 80-dBFS for a 12-bit ADC. This technique can also be used for offset error correction. Such an improvement at the cost of an additional identical

ADC and with some extra DSP circuitry looks promising.

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