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High-Efficiency Power Amplifier for Wireless Sensor Networks

Devrim Aksin

Department of Electrical Engineering
University of Texas at Dallas
Dallas, Texas, USA
devrim.aksin@ieee.org

Stefano Gregori

School of Engineering
University of Guelph
Guelph, Ontario, Canada
sgregori@uoguelph.ca

Franco Maloberti

Department of Electronics
University of Pavia
Pavia, Italy
franco.maloberti@unipv.it

Abstract— We designed a high-efficiency class-E switched-mode power amplifier for a wireless networked micro-sensors system. In this system, where each sensor operates using a micro-battery, has local processing capability, and contains on the same chip integrated sensing elements and a RF transmitter, most of the power is dissipated by the transmitter. The proposed amplifier achieves 92.4% maximum drain efficiency and can vary the transmitted power between -4.2 to -0.2 dBm with almost constant efficiency. This last feature is obtained by controlling the modulation duty cycle and by switching the capacitors' values in the parallel circuit. The possibility of choosing the transmitted power depending on the distance from a base station or other sensors and on the charge level of the battery, combined with power aware network protocols, improves network lifetime, reliability, and adaptability. The amplifier is designed in $0.18\text{ }\mu\text{m}$ CMOS process and operates with nominal 1.2 V supply.

I. INTRODUCTION

The integrated circuit technology, supporting the ongoing miniaturization of sensing, processing, storage, and transmission, enables new kinds of embedded systems. These systems are distributed and deployed in environments where conditions change dynamically. They comprise a collection of devices, each acting as a node of a physical communication network collecting and disseminating a wide range of environmental data.

Low data rate sensor networks are rapidly emerging as a major new player in the information technology arena. Currently many research efforts focus on the design of small, low-cost, lightweight, fully integrated, wireless communication sensor nodes. The network lifeblood, fueling range, versatility, and reliability, comes from the available power sources and from the efficiency in their usage. Each node has a battery or an energy storage device and may have means of extracting energy from the environment (solar, vibration, temperature difference) [1] or receiving wirelessly transmitted energy from a base station [2].

Figure 1. Block diagram of the micro-sensor.

Physical dimensions and cost of energy extraction/storage devices, limit the node power budget to a level somewhere below $100\text{ }\mu\text{W}$ to have a reasonable network lifetime [2], [3]. In nodes organized as in Fig. 1, the most power-hungry block is the transmitter, which generally uses more than 50% of the available power.

Considering power dissipation, the key component in the whole sensor node is the power amplifier (PA). The challenges faced in designing a power amplifier for wireless sensor networks are quite different with respect to its counterpart of conventional wireless transmitters (e.g. Bluetooth, Wi-Fi). Here the power constraints typically limit transmission duty cycle to less than 1%, so that occasional bursts of data packets are sent with a low data rate (a few tens of Kbit/s) to neighboring nodes or to a base station in a few tens of meters range. Power efficiency is the most important requirement, which directly affects network range, lifetime, and reliability. In addition a power control circuit must be designed in order to change the output power for various transmission distances, variable fading conditions, and charge level of the battery. Finally, since the power amplifier must be off when idle and turned on just for short transmission bursts, the turn-on transient must be very fast to reduce the overhead power dissipation.

In this paper we present a high-efficiency class-E switched-mode power amplifier suitable for wireless

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networked micro-sensors systems. Switched-mode power amplifiers have a better efficiency than linear amplifiers (A, B, A/B), thus a non-linear modulation scheme (i.e. FSK) is the best choice for low-power consumption. In addition the proposed transmitter uses the 433 MHz ISM band, which gives a shorter path-loss than higher frequencies, allows more power-efficient transmitter circuits, and still provides enough bandwidth for the transmitted signal and allows the design of a relatively small antenna. The amplifier, together with the power control circuit, has been designed in 0.18 μ m CMOS process and operates with nominal 1.2 V supply.

The first part of the paper describes design issues and trade-offs. The following section discusses simulation results and the last section offers our concluding remarks.

II. DESIGN CONSIDERATIONS

A. Approach

The schematic and circuit waveforms of a class E tuned amplifier are shown in Fig. 2. It consists of a transistor (M1), operated as a switch, an inductor L_0 , large enough that the current through it can be considered almost constant, and a parallel load network (L - C - R_A - C_1). The signal V_{IN} is a square waveform generated by the preamplifier, which turns on and off M1 at the operating frequency (433 MHz). The circuit is characterized by two resonant frequencies: when M1 is on, the series-resonant circuit consists of C , L , and R_A ; when M1 is off, consists of C_1 , C , L , and R_A . For optimum operation (i.e. minimum power dissipated by M1), the drain voltage V_D and its derivative dV_D/dt must be zero when M1 turns on (at $\omega t = 2\pi$).

Fig. 2 shows possible current and voltage waveforms for optimum operation. This condition, for a given operating frequency, is met by setting the values of C_1 , C , L , and R_A , and by choosing a proper duty cycle. A detailed analytical model for the circuit and the derivation of the steady-state waveforms are described in [4].

Figure 2. Power amplifier and circuit waveforms.

Figure 3. Duty cycle vs. output power.

Figure 4. Voltage waveforms for variable output power levels.

The output power of the circuit is related to the waveforms, which in turn depend on V_{DD} , the operating frequency, the duty cycle, and the values of C_1 , C , L , and R_A . The variation of any of these parameters affects the output power, but, in general, drives the working conditions away from the maximum efficiency point.

Changing the output power, while keeping the conditions for maximum efficiency, requires the simultaneous variation of more than one of the mentioned parameters. Parameters that can actually be changed in an integrated circuit are the duty cycle (that can be accomplished by the preamplifier, Sec. II.B), the capacitor C_1 (additional capacitors can be connected in parallel using n MOS switches), the resistor R_A (which in practical applications results in a matching network, whose input impedance depends on the values of capacitors that can be varied the same way as C_1 , Sec. II.C).

The values of the parameters corresponding to any desired value of output power can be calculated starting from the equation describing the steady-state waveform for V_D and applying the optimum turn-on conditions ($V_D = 0$ and $dV_D/dt = 0$). Figs. 3, 4, and 5 present results from numerical simulations. Fig. 3 shows the required duty cycle for maximum efficiency when the output power ranges from 0.4 to 6.4 mW. Drain voltage waveforms corresponding to different output power levels (0.4, 1.2, 3.2, 6.4 mW) are plotted in Fig. 4.

The same parameters variation can also be used to maintain a constant output power while V_{DD} changes (for example because of battery discharge). Fig. 5 presents voltage waveforms for a constant output power (1.2 mW), and $V_{DD} = 0.8, 1.2$, and 1.6 V.

Figure 5. Voltage waveforms for constant output power and variable V_{DD} .

Figure 6. Duty cycle modulator (DCM).

B. Preamplifier with Duty Cycle Adjustment

The duty cycle adjustment of carrier frequency is obtained using the circuit shown in Fig. 6. The pulse is adjusted with a variable resistor created by pass transistors M1-M2 and control voltages. The circuit works as follows, whenever a rising edge occurs at the input, the output of DFF starts rising, this voltage is applied to the input of the inverter INV1 with an RC delay, determined by the on resistance of the pass transistors and the input capacitance of the inverter. Then, INV1 resets DFF. Hence the pulse width is determined by the propagation delay from DFF's Q terminal to INV1's output terminal plus DFF's reset terminal to Q terminal. Fig. 7 shows the variation of the duty cycle with respect to the applied control voltage. The transient simulation results showing the output of the duty cycle modulator is given in Fig. 8. The circuit dissipates 170 W at 433 MHz. Although, it is not shown here, digital programming of the RC delay line is also possible. For the digital programming scheme, transistors M1 and M2 are designed as multi finger pass transistors that can be turn on or off digitally so that effective channel width of the pass transistors can be programmed.

C. Capacitively Programmable Load

In order to change the equivalent resistive load with respect to different output power (or equivalently duty cycle setting), a capacitively programmable load is designed. The whole class E power amplifier schematic is given in Fig. 9, and capacitively programmable load consists of the components C_2 , C_3 , L_1 , and R_A . The real part of the power

amplifier's load in proximity to the resonance frequency can be expressed as:

$$R_L = \frac{R_A}{1 + (R_A^2 L_1^2 - 2L_1 C_3)\omega^2 + L_1^2 C_3^2 \omega^4} \quad (1)$$

As it is clear from (1), effective load near the resonance frequency can be modified using C_3 . Since, changing the value of C_3 changes also equivalent resonance frequency of the load, the value of another capacitor, i.e. C_2 , is changed in correlation with the changes of C_3 so that overall resonance frequency can be set at the desired 433 MHz.

Figure 7. The variation of the duty cycle with control voltage.

Figure 8. Transient simulation result of the duty cycle modulator.

Figure 9. Circuit schematic of the power amplifier.

Figure 10. Drain voltage of switch transistor M1 (PSS analysis).

Figure 11. Drain voltage of switch transistor M1 (transient analysis).

III. RESULTS

To prove the validity of the proposed scheme, the class-E power amplifier shown in Fig. 9 has been extensively simulated. Table 1 shows the obtained output power and power added efficiency of the class-E power amplifier for different C_1 , C_2 , C_3 and duty cycle values. Fig. 10 shows the drain voltage of the switch transistor M1 for the output power level of -0.211 dBm obtained using periodic steady state analysis (PSS). Fig. 11 shows the initial transient at the switch drain terminal. The power added efficiency of the class-E amplifier, together the PAE of the whole power amplifier including the duty cycle modulator with respect to the output power is shown in Fig. 12. Class-E power amplifier shows more than 87% throughout the whole output power range and of course overall PAE decrease with the decrease of the output power because of the constant power consumption of the duty cycle modulator (DCM).

Figure 12. Power Added Efficiency (PAE) of the class-E power amplifier: a) alone; b) with preamplifier, i.e. duty cycle modulator.

IV. CONCLUSION

Wireless sensor networks set new challenges in designing low-power communication circuits. The power available to each micro-sensor node is a vital resource for the functioning a sensor network and the transmitted power is a substantial part of it. This paper presents a high-efficiency power amplifier, which is particularly well suited for wireless networked micro-sensors systems. Simulation results shows that it keeps optimum efficiency conditions, with PAE over 87%, while delivering variable output power, from -4.262 to -0.211 dBm, without needing for additional power control mechanisms.

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TABLE I. OUTPUT POWER AND POWER ADDED EFFICIENCY FOR DIFFERENT COMPONENT VALUES AND DUTY CYCLE

Duty Cycle	L [H]	C [F]	C_1 [F]	L_1 [H]	C_2 [F]	C_3 [F]	Output Power [dBm]	Power Added Efficiency [%]
0.178	1.00E-07	6.50E-11	1.25E-12	9.19E-09	2.16E-11	2.48E-11	-4.262	92.46
0.205	1.00E-07	6.50E-11	1.20E-12	9.19E-09	2.20E-11	2.81E-11	-3.075	92.44
0.230	1.00E-07	6.50E-11	1.15E-12	9.19E-09	2.20E-11	3.05E-11	-2.153	91.10
0.253	1.00E-07	6.50E-11	1.10E-12	9.19E-09	2.19E-11	3.24E-11	-1.407	90.40
0.275	1.00E-07	6.50E-11	1.05E-12	9.19E-09	2.18E-11	3.41E-11	-0.741	89.42
0.296	1.00E-07	6.50E-11	1.00E-12	9.19E-09	2.16E-11	3.56E-11	-0.211	87.94