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DESIGN OF ULTRA LOW-POWER ANALOG CELLS WITH DYNAMIC CURRENT BIASING

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ABSTRACT

This paper describes design strategies for ultra low-power analog cells. It is assumed that the circuits are used in sampled-data systems with only capacitors and switches. The operation requires large currents to quickly charging or discharging capacitors and, after a transient, a very small quiescent current. The proposed strategy uses dynamically controlled bias current that leads to a very low average power consumption while the slew-rate and frequency response is good enough. Two categories of circuits are discussed: low-voltage *OTA* and comparators. For both circuits simulation results confirm the validity of the basic idea and show good performances with average currents in the sub micro-ampere range.

1. INTRODUCTION

The increasing importance of analog interfaces for portable applications pushes power consumption to lower and lower levels. The goal is achieved by decreasing the voltage supply and by minimizing the bias current in analog cells [1],[2],[3]. However, reducing the bias current diminishes the bandwidth of the signal and the capability of driving loads. Since the analog cells are normally used for sampled-data circuits (like switched capacitor filters or data converters) the main limit to a current reduction comes from the reduced driving capability of capacitances. At the beginning the charging or discharging of capacitors needs large currents; when the capacitor is almost charged the bias current can go to zero. Consequently, the design of analog cells with ultra-low power consumption cannot rely on the commonly used approach in which the bias current is constant. More conveniently it is necessary to provide current when it is necessary. It is therefore useful studying new methods that foresee bias currents that change dynamically according to the necessity of the analog cells and its load.

A given *dc* bias current, I_B , made available by the slewing of an *OTA* charges a capacitance C_L with a slew rate given by $\Delta V/\Delta t = I_B/C_L$ until the output and the feedback network bring the input differential voltage into the region of normal operation. Then, the output voltage evolves almost exponentially controlled by the gain-bandwidth of the *OTA* used. For ultra-low currents the region of normal operation is very small (depending on the transistor sizing it can be few *mV* or ten of *mV*) and the time transient of the output signal is almost dependent on the slewing phase only.

Assume that the voltage across a capacitor evolves exponentially with a given time constant, τ . The charging current also changes exponentially

$$I_C(t) = V_C(\infty) \cdot C(1 - e^{-t/\tau}) \quad (1)$$

therefore, if the bias current leading to the slewing limit changes exponentially as equation (1), the slewing will lead to an exponential charging as it is for the control of an *OTA* with a large bias current.

This paper discusses on the design of analog cells controlled by dynamic bias current. The goal is to speed up the charging of capacitors and to mimic the operation of analog cells with a large bias current.

2. DYNAMIC CURRENT BIASING

Main bias current and a number of current mirrors determine the biases of analog cells. Fig. 1 shows a typical solution used. A main generator drains current from a diode-connected transistor. The aspect ratio of mirroring transistors increases or reduces the current in the various branches but leads to constant values. The situation is not the optimum for capacitive loads or when using capacitances in feedback connection. As already mentioned in the introduction it would be necessary to use currents that are large at the beginning of the switching phase and decrease exponentially to a low value (or at the limit zero).

Fig. 1. Conventional current bias.

Fig. 2 shows two possible solutions that enable a dynamic control of the bias current. Both are based on the charging transient of a capacitance. The circuit in Fig. 2 a) (Type I) enables using the charging current directly on a circuit. The circuit of Fig. 2 b) (Type II) mirrors the charging current of a capacitor for a use in different parts of the analog cells. The capacitance is discharged during phase 1 and it is charged through the resistance of the switch (and the diode connected *MOS* for Type II) during phase 2. Possibly, an extra resistance can be used in series to the circuit. The time

constant and the peak current are determined by the components values.

Fig. 2. Dynamic current biases.

The use of a dynamic exponential bias current can be combined with an ultra-low dc term that possibly ensures a minimum bandwidth in the quiescent mode. This compensates for noise fluctuations and leakage currents.

3. ULTRA LOW-POWER OTAs

The design of *CMOS OTAs* with currents below $1\mu A$ benefits from the operation of *MOS* transistors in the sub-threshold region. The drain current changes exponentially with the gate voltage as it happens for bipolar transistors. For a given bias current the transconductance is maximized and the small signal gain of the stage is large. Thus, single stages amplifiers can obtain a gain in the order of 45-55 dB that is enough for many ultra low-power applications.

The use of a cascode stage would give higher gain but the output dynamic range diminishes by at least two saturations. The use of a two-stage architecture is also good for enhancing the gain but the required pole splitting compensation can be a limit for enhancing the slewing with a dynamic biasing solutions.

Fig. 3. Single stage amplifier.

The use of low voltages demands for output stages with large dynamic range. An inverter with active load is the solution normally required. Thus, for low-voltage a suitable *OTA* architecture is the one shown in Fig. 3. The common-mode feedback is not shown. It can be implemented with a switched capacitor circuit. The scheme of Fig. 3 has a limit to very low voltage. The V_{DS} of the input pair is $V_{DD} - V_{GS,p} - V_{sat,n}$. In order to have a good V_{DS} it is not recommended to have V_{DD} lower than $0.8V$ (with thresholds of both transistors at around $0.4V$). The schematic in Fig. 4 achieves a lower minimum supply voltage. The use of the folded branch gives more room for V_{DS} of the input pair.

Thus, the scheme can work down to V_{DS} as low as $0.6V$. The p-channel bias generators of the input stage serve both the input differential stage and the folded branches. The voltage of the diode-connected transistor is the input of the inverters with active loads at the outputs. The cost of a minimum supply voltage is an increase by 50% of the used current.

Fig. 4. Modified single stage amplifier.

4. SIMULATED PERFORMANCES

The circuit of Fig. 4 has been simulated at the transistor level using a *CMOS 0.18μm* technology and $V_{DD} = 1V$. The value of the bias current I_B is as low as $25nA$. The total dc current consumption is therefore $200nA$. The small signal response of the *OTA* under these operative conditions leads to a dc differential gain $A_{dc} = 48dB$ and $f_T = 160kHz$. The phase margin with a load of $0.5 pF$ is more than 80° . Fig. 5 shows the Bode plots.

Fig. 5. Bode plots of the differential gain (total current $0.2\mu A$).

The obtained dc gain can be satisfactory for some ultra low-power applications. However, the speed of the circuit limits the use to very low clock frequencies. The use of dynamic current biases (Type II) in parallel to *Mp1-Mp4* improves significantly the dynamic performances. The circuit in Fig. 6 helps in estimating the effect of the bias current boost.

The input differential signals change by $200mV$ and the output is expected to change by $200mV$ as well. The response has been simulated with and without the dynamic current biases. The “Type II” reference is obtained by charging a $0.4 pF$ capacitance through a diode connected transistor which aspect ratio is equal to *Mp1* ($=1/2 Mp2$).

Fig. 6. Test-bench for determining the transient response of the OTA of Fig. 4 with and without dynamic current biases.

Fig. 7 shows the responses in the two considered cases. The slew rate with the static current bias is $16V/ms$ a little less than what expected ($25V/ms$). Thus, it takes more than $40\mu s$ to settle to the final value. With the dynamic current bias the response is very fast: in less than $0.1\mu s$ the output reaches the 3% the final value. Then, the signal obtains an accuracy better than 1% in $5\mu s$.

The simulation results show that the circuit with dynamic current bias operates properly with a clock of $100kHz$. The circuit without dynamic current bias achieves the same performances with a total current consumption of $1.8\mu A$, 9 times the initial value of dc current. Actually, the pulse of bias current corresponds to an average increase of the dc bias. The integral of the current pulse resulting from the given simulation is $3.4 pCoul$. The average current over $10\mu s$ is $340pA$ that added to the dc term ($200pA$) leads to $540pA$, less than $1/3$ of the current required to obtain the same performances with a static biasing. If the clock frequency is reduced to $50kHz$ the static current becomes $1000pA$ while the average current with dynamic biasing becomes $(200+170)=370pA$ still almost $1/3$ of the static counterpart.

Fig. 7. Output responses with and without dynamic current biases. The supply voltage is 1V and the analog ground is 0.5V.

The dynamic current biasing obtains an optimum for given design conditions. If the current boost is not enough the output voltage swing is slow. If the boost is too large the output swing exercises an

overshooting. The results of transistor level simulation with three different cases are shown in Fig. 8.

Fig. 8. Output responses of the OTA of Fig. 4 with 0.2pF, 0.4pF and 0.8pF in the Type II current boost generator.

The three curves correspond to a capacitor of $0.2pF$, $0.4pF$ and $0.8pF$ in the scheme of Fig. 2 b). The difference between the curves is significant. However, the used capacitances are $1/2$ and 2 times the optimum value.

5. ULTRA LOW-POWER COMPARATOR

The dynamic current biasing technique can be also used for designing the pre-amplifier stage used in medium accuracy comparators. If the required resolution is some ten of mV the comparison function can be obtained with a latch. For higher accuracy the control of the latch must be enhanced with a gain that often is in the range of ten or one hundred.

Fig. 9. a) Dynamically current biased pre-amplifier with dynamic voltage bias. b) Low power latch.

Fig. 9 a) shows the proposed circuit schematic of a medium gain pre-amplifier. The current in the scheme is given by the "Type I" solution of Fig. 2 a). Two

non-overlapped clock phases control the circuit. During phase Φ_1 all the capacitors are discharged. The two transistors M_3 and M_4 are off. During phase Φ_2 capacitances C_3 and C_4 establish the voltage $V_{DD}C_3/(C_3+C_4)$ at the gate of M_3 and M_4 . The result is a dynamic generation of a voltage bias. Therefore, M_3 and M_4 operate like a switch during one phase and during the other phase they set up cascode configurations along with the input transistors. The charging of capacitors C_1 and C'_1 provides the current to the circuit. M_5 and M_6 limit the total charging current and operate as common mode feedback. In the steady state conditions the output voltages goes both down to the threshold of M_5 and M_6 . However, unbalanced inputs determine different transient responses: one of the outputs goes down faster than the other, thus establishing a differential gain that varies with time.

Simulations show that 2 mV differential input produces a differential output larger than 30 mV for a relatively long time-interval. Then the voltages drop down. Therefore, within a given a time-interval the pre-amplifier gain is more than 23 dB.

Let us estimate now the energy required by the circuit. Each comparison requires to charge the series connection of C_3 and C_4 and to charge C_1 and C'_1 to the V_{DD} minus the output voltage. Therefore, the maximum energy for comparison is

$$E_{\max,comp} = \frac{1}{2} \left[\frac{C_3 C_4}{C_3 + C_4} V_{DD}^2 + (C_1 + C'_1) (V_{DD} - V_{th})^2 \right] \quad (2)$$

using 0.2 pF for C_1 , C'_1 and $C_3 = 0.1$ pF, $C_4 = 0.3$ pF, $V_{DD} = 1.2$ V and $V_{th} = 0.6$ V it results $E_{comp} = 0.126$ pJ.

The latch of Fig. 9 b) requires 8 mV at the input for avoiding meta-stability. Moreover, the expected input random offset is 7 mV. Therefore, the required driving is less than 20 mV. Transistor sizing suitable for a 2MHz strobe determine energy consumption per cycle as low as 0.1 pJ. For a lower speed the latch energy will be lower. Summing up the total energy per comparison is 0.226 pJ when the circuit operates at 2MHz. The corresponding power consumption of the entire comparator is 0.45 μ W at 1.2V supply.

A possible use of the above-described comparator is in a data converter. The successive approximation algorithm is suitable for low power. Fig. 10 shows a possible scheme that uses the charge redistribution method and only one comparator. The power consumption of the circuit depends on the switching of the capacitors and the comparator.

Fig. 10. Circuit diagram for a successive approximation converter,

The comparator scheme of Fig. 9 has been used in the SAR ADC to obtain 8-bit of resolution [4]. The simulation results are shown in Fig. 11. The top plot is the signal at the output of the pre-amplifier. It can be observed that when the differential input (bottom plot) is large the outputs remain apart significantly. However, even when the differential input is small the outputs drop with different slopes and at the end of the period we observe some gain. The control of the successive approximation register (SAR) leads to the expected waveform at the input of the pre-amplifier.

Fig. 11. Simulation results for the ADC (a) output signals of the preamplifier (b) (c) differential output signals of the latch (d) input signals of the comparator.

Fig. 12 verifies the operation of the latch with the foreseen energy budget. When the latch control goes on the two outputs goes in the proper direction with an input difference of 10 mV.

Fig. 12. Response of the latch with 10 mV at the input.

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