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Low-Power 6-bit Flash ADC for High-Speed Data Converters Architectures

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Abstract—The design of low-power, medium resolution flash converter is presented. The goal is to provide a basic cell with state-of-the art figure of merit thus permitting low-power data converter architectures with a more flexible use of flash ADC cells. The designed 6-bit flash uses interpolation and V/I converters that operate as preamplifier stage of latches. Circuit simulations show a figure of merit as low as 1.2 pJ/conv-lev at 100-MS/s sampling frequency and 3.3-V analog supply voltage.

I. INTRODUCTION

The design of low-power data converters requires a proper use of the power budget. The conversion algorithm and the architecture are often determined by the power required by basic blocks. For example, a pipeline converter utilizes flash ADCs and residual generators. The number of bits in the last stage is determined by the power of the used flash. Also, the number of bits of intermediate stages comes from a trade-off between the need of extra stages and the increased power request of flash and residual generator. For a multi-bit O-th order sigma-delta the resolution increases by $(O+1/2)$ -bit per doubling of the sampling frequency. However, an increased clock frequency augments the power consumed by the OTAs. The use of more bits in the modulator can be more power effective if the extra power required by the flash is less than the equivalent power increase in the OTAs.

Flash converters with medium-high resolution are not power effective solutions. An N -bit converter uses 2^N comparators. If the reference voltage is large and the number of bits is small the quantization step is several tens of mV. A simple latch can realize the comparison and the consumed power is relatively low. On the contrary, when the quantization step is 20-30 mV or less it is necessary to use a preamplifier before the latch; the speed requirements lead to a significant increase of the power consumption. Thus, for modern circuits with 1.5-V supply voltage or less the reference of the ADC is few hundred of mV and for 4 bits or more it is necessary to use comparator preamplifiers. The figure of merit (FoM) of this kind of flash converter is larger than 7 pJ/conv-lev: a 6-bit 100-MS/s ADC would require a power consumption equal to 22 mW.

The above considerations motivate this paper. Its goal is to identify power effective flash architectures capable to obtain FoM lower than 1.5 pJ/conv-lev. The designed circuit is a 6-bit 100MS/s ADC with a total current consumption equal to

2.5 mA. The supply voltage is 3.3 V giving 1.2 pJ/conv-lev, about a factor 5 less than other published works.

Another important design parameter is the supply voltage. It depends on the technology and the specifications of the data converter or, in some case, the system that uses the data converter. A strategy that minimizes the power consumption foresees using different supply voltages for the analog and the digital section. The method is beneficial but the analog-digital interfaces can be problematic. This paper assumes that the analog part uses 3.3 V while digital circuits utilize 1.8 V.

The paper is organized as follows. In Sect. II the principles of interpolation are briefly reviewed, while in Sect. III the design of the ADC is described in detail, considering each basic building block (V/I converter, interpolation stage, latch). Sect. IV reports the simulation results of the flash ADC implemented at a fully-transistor level in a standard 0.35- μ m CMOS technology with a supply voltage of 3.3 V.

II. THE INTERPOLATION PRINCIPLE

Flash ADCs identify the quantization interval that contains a given input value by comparing the input signal with all the thresholds [1]. In an N -bit full-flash ADC the required number of comparator is equal to $2^N - 1$. Therefore, the current consumption associated with the comparator blocks increases exponentially with the number of bits.

The use of interpolation possibly reduces the power consumption. The number of input pre-amplifiers is reduced by the interpolation factor. They generate a signal equal to the input voltage V_{in} minus the coarse thresholds. As a matter of fact the remaining levels are obtained with an interpolation between the output of two successive gain stages. The output of each pre-amplifier is the linear amplification of the differential input for a given input range. Then, the output saturates at an upper or lower clipping level. Two successive preamplifiers have an overlapped region where the responses are non-saturated. As a consequence the use of an interpolation circuit generates a response with zero crossing midway between the zero-crossing of the preamplifiers. A set of latches detects the crossing points and provides a thermometric code at the output of the ADC.

The use of interpolation is beneficial for low-power consumption and for reducing the input capacitive load. The principle can be applied using voltage signals or current signals. However the use of voltage signals is difficult in a

Fig. 1. Circuit diagram of the voltage-to-current converter.

CMOS implementation since in order to have interpolation the preamplifiers have to drive a resistance network [2]. On the other hand the use of current is more suitable as the interpolation circuit can be realized easily by summing the current at the output of the preamplifier stages with different weights.

III. LOW-POWER FLASH ADC ARCHITECTURE

The pre-amplifier function for the interpolator is obtained by a set of 18 (9 per input) voltage-to-current converters that cover the available dynamic range, which in our case goes from 1.15 V to 2.15 V. The input signal is supposed to be differential around the analog ground (equal to 1.65 V with a supply voltage of 3.3 V). The differential voltage input swing is ± 1 V, while the coarse differential quantization step is ± 125 mV differential. The interpolation by a factor of 8 within each coarse interval will lead this value to about ± 15 mV, for a total resolution to 6 bits (65 thresholds levels). The flash ADC uses a fully-differential architecture to achieve an high rejection of the common mode disturbances.

A. V/I converter

Fig. 1 shows the scheme of the used V/I converter [3]. The positive input of the block is one of the reference voltage generated by a resistive string divider, while the negative one is a single-ended input. The current in the input p-channel devices M1-M2 is given the current sources M3-M4 (with a current of 6 μ A). The output current determined by the cascodes M5-M7 and M6-M8 is the difference between the currents drawn by the current sources M9-M10 (equal to 12 μ A) and M3-M4. As a result, when the two input V_+ and V_- are at the same level, the current in R is zero, being the circuit fully balanced, and the output currents are both 6 μ A. A local feedback loop ensures that the current in the input p-channel devices is kept constant and equal to the biases M3-M4.

The input voltage is followed by the voltage across R. Therefore the current flowing across the resistor is provided by the cascode output current sources. If the currents on the output branches are I_+ and I_- , in the linear region they are

Fig. 2. Output currents of the V/I converter with large input swing.

given by

$$I_+ = I + V_{in,diff}/R \quad (1)$$

$$I_- = I - V_{in,diff}/R \quad (2)$$

where I is the 6 μ A quiescent output current.

Two clamping transistors (M11-M12) prevent that one of the output currents goes to zero when the V/I is fully unbalanced (i.e. the negative input is below or above the reference voltage by more than 300 mV). This gives a fast recovery time from fully unbalance. Fig. 2 shows the output currents for input swinging from the lowest input voltage (1.15 V) to 1/2 LSB above the threshold voltage. The currents never goes to zero thus obtaining a fast crossing despite the big previous overdrive: it is equal to about 2 ns which allows the following latches to fast preset the analog input.

Fig. 3. Voltage-to-current transfer function of V/I converters connected to two successive threshold voltages.

Fig. 3 shows the transfer function of two V/I converters connected to two different threshold voltages. The response with large signals is non-linear but the used region is linear enough for our purposes. Mirrored replicas of the output currents of the V/I converters are delivered to the following interpolation stages.

Fig. 4. Use of the voltage to current converters.

B. Current interpolator stages

One half of the V/I converters serve the positive single-ended input, while the remaining ones are assigned to the negative one, as indicated in Fig. 4.

The differential output currents of the V/I converters are used as input for the 8 interpolator stages. Each interpolator stage is composed by eight sections which must provide the interpolated threshold levels.

As indicated in Fig. 5 the first section mirrors the currents coming from the first positive V/I converter and first negative one. The currents are then summed together in a way that we have on one input of the latch the current $I_{p,1+} + I_{n,1-}$, while on the other we have $I_{p,1-} + I_{n,1+}$. The current latch must distinguish if the differential current $I_{diff,p,1} = I_{p,1+} - I_{p,1-}$ from the first positive V/I converter is greater than the differential current $I_{diff,n,1} = I_{n,1+} - I_{n,1-}$ from the first negative one. As a consequence the latch detects if the input differential signal exceeds the first threshold.

The second section uses 7/8 of the current of the first V/I converters and 1/8 of the current of the second V/I converters. The different weights in the current summation are implemented simply varying the number of fingers of the transistors realizing the mirrors. In this case the current latch

Fig. 5. Circuit diagram of the interpolator stage.

must decide if the following relationship is verified:

$$\frac{7}{8}I_{diff,p,1} + \frac{1}{8}I_{diff,p,2} > \frac{7}{8}I_{diff,n,1} + \frac{1}{8}I_{diff,n,2}. \quad (3)$$

That happens if the input differential voltage is greater than the second threshold, which is not one of the levels of the resistive string as it has been obtained with an interpolation.

The group of summing stages ends with the section which uses 1/8 of the current of the first V/I converters and 7/8 of the second V/I converters. Note that in order to enhance the output impedance of the current mirrors a cascode transistor is added before the latch inputs.

C. Current latch

Fig. 6 shows the scheme of the current latch. During the latching phase (indicated as Φ_1), the switches S_1 and S_2 are closed and the latch is pushed to one state or the opposite one according to which current between I_1 and I_2 is the greatest one. During the reset phase (indicated as Φ_2) the latch is opened and the two n-channel devices act as diode-connected loads for the current sources I_1 and I_2 . The supply voltage of the current latch is 1.8 V. In addition to a lower power consumption the circuit is able to keep high the speed of operation: after the latching phase the comparison between

Fig. 6. Scheme of the current latch.

the two currents makes the voltage of one of the two output nodes equal to V_{DD} of the digital section (1.8 V). This avoids to turn off the input current source: it is a flow from the 3.3 V supply to the 1.8 V supply. Keeping the transistor that generate that current in saturation avoids a possible recovery from off to on and enhances the speed performances. Also, the method reduces the glitches in the interpolated currents.

IV. SIMULATION RESULTS

The proposed flash ADC has been simulated at the transistor level using a 0.35- μm CMOS technology with a supply voltage of 3.3 V for the analog part and 1.8 V for the digital part.

The static linearity is simulated with an input ramp sampled at full speed. The differential non-linearity (Fig. 7) and the integral non-linearity (Fig. 8) with equal resistors in the divider used for generating the references are less than 0.2 LSB. Dynamic behavior tests use a clock frequency equal to 100 MS/s and a full-scale input sine wave at 30 MHz. The resulting spectrum is shown in Fig. 9. The resulting signal to noise and distortion ratio is 36.2 dB, which means an effective resolution of 5.7 bits. The overall current consumption is 2.5 mA, giving a dissipated power of 8.25 mW. The FoM is 1.2 pJ/conv-lev. The value is much lower than previously published results. Moreover, a reduction of the supply voltages by 45% (from 3.3 V to 1.8V) would lead to a sub pJ/conv-lev, excellent figure for flash architectures.

V. CONCLUSION

A 6-bit 100-MS/s flash ADC has been presented. The number of comparators with respect to conventional flash ADC architectures is reduced thanks to the use of interpolation. The currents coming from the input V/Is are combined and give 8 interpolated thresholds for each starting coarse quantization interval with minimum power consumption. Transistor level simulations confirm the effectiveness of the proposed design, with an effective number of bits equal to 5.7 for an input frequency of 30 MHz and a sampling frequency of 100 MS/s, with a current consumption limited to 2.5 mA.

Fig. 7. Differential non-linearity at 100-MS/s sampling frequency.

Fig. 8. Integral non-linearity at 100 MS/s sampling frequency.

Fig. 9. Output spectrum at 100 MS/s with a 30-MHz full-scale input tone.

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