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Design of a Current Mode 6-bit 100 MS/s Flash A/D Converter with 0.75 pJ/conv-lev FoM

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Abstract – The design of a low-power 6-bit flash A/D converter with state-of-the-art figure of merit for flash architectures is presented. The target resolution with the lowest power consumption is achieved by using the voltage-to-current conversion strategy. The sampling frequency is 100 MHz and the proposed converter is able to work with an input signal frequency very close to Nyquist rate. Considering that the analog and the digital supply voltages are 1.8 V and 0.9 V, respectively, the achieved figure of merit is equal to 0.75 pJ/conv.

I. INTRODUCTION

The recent trend is using portable systems embedding data converters with an increasing conversion rate and medium/high resolutions. In addition to the required speed and accuracy, it is important to achieve very low power consumption, normally estimated using the figure of merit (FoM). The architectural choices often depend on the availability of suitable micro-blocks. Thus, for example, the number of levels in a multi-bit sigma-delta architecture depends on the power effectiveness of the flash and on the linearity provided by the DAC. Also, the number of bit in various stages of a pipeline architecture (especially the ones of the last stage) are determined by the power effective of the flash schemes. Indeed, the power consumed by each pipeline stage is given by the power needed by the flash and the one of the op-amp used for the residual generation. Therefore, it may be convenient using multi-bit power effective flashes replacing the last two or three stages of the pipeline architecture.

The above considerations motivate this study that, obtaining a FoM similar or better than power effective counterparts, makes the designed flash an useful stand-alone solution and a valuable macro-block to be used in data converter architectures [1], [2]. Notice that the best reported flash A/D converter with more than 5 bit achieves a FoM of about 2 pJ/conv [3]. Unfortunately, the result, albeit significant, is not suitable for the use in novel data converters

architecture by competing with two-step or pipeline solutions that, as known, cost latency.

The low supply voltage of modern CMOS technologies leads to references in the 1 V range. Therefore, with 6-bit the quantization step is about 16 mV, value that is critical as it is not enough for above directly driving a latch. Therefore, it would be necessary using preamplifiers that consume power. This design overcomes the problem by using a current domain solution. The scheme suitably uses, as it will be described in details shortly, V-to-I converters and interpolation for optimizing the use of power. In order to further reduce the power, the scheme exploits the possible availability in integrated systems of multiple supplies. In particular, this flash A/D converter uses for the analog and the digital parts 1.8 V and 0.9 V, respectively.

The paper is organized as follows. Section II describes the chip architecture. Basic building blocks (V-to-I, common mode feedback network, interpolation and latch stage) are described in Section III. Section IV reports the simulation results at the transistor level. The A/D flash uses a 0.18- μ m CMOS technology for achieving a total power consumption of 4.6 mW. The DNL and INL are both below 0.25 LSB.

II. CHIP ARCHITECTURE

Fig. 1 shows the architecture of the 6-bit A/D low power flash. A resistive divider provides the required voltage references, referred to as V_{refi} ($i = 1, \dots, 17$), to the V-to-I stage with 62.5 mV step between two consecutive references (4 LSB). The front end is made by 17 V-to-I stages which convert the input from the voltage to the current domain. The structure is fully differential and the input ranges from 0.4 V to 1.4 V with analog ground at 0.9 V. The differential V-to-I outputs are then transformed into voltage by equal resistors R whose value ensures enough differential amplitude for the following *Latch and Interpolation Stage*.

The required 64 levels are attained by interpolation by 4 of the V-to-I outputs similarly. The operation is made directly at the input nodes of the latches, as explained in the next Section. A possible problem resulting from the used scheme is the sensitivity to the common mode signal and for this a suitable scheme that ensures a good CMM rejection (the block *V-to-I CMF* in Fig. 1) provides a control signal for all the V-to-I schemes.

Figure 1. Block diagram of the proposed converter.

III. BASIC BUILDING BLOCKS

A. V-to-I

Fig. 2 shows the V-to-I converter. It is a variation of the solution proposed in [4] for meeting the accuracy request and obtaining good Montecarlo simulation results. NMOS transistors M_9 and M_{10} , whose sources are connected by means of resistor R_7 , compose the input pair. P-channel transistors M_1 - M_2 , M_3 - M_4 , M_5 - M_6 , and M_7 - M_8 together with n-channel transistors M_{13} - M_{14} and M_{15} - M_{16} implement current mirrors. To improve mirror accuracy and linearity all current mirrors have been realized by cascode structures. The bias voltages V_{CMFPj} ($j = 1, \dots, 4$) and V_{CMFNm} ($m = 1, \dots, 4$) are generated in *V-to-I CMF* block of Fig. 1 and discussed in the following of this Section. Bias voltages V_{B1} and V_{B2} are also generated in the bias stage. Current mirrors made by transistors M_1 - M_2 , M_7 - M_8 , generate $10 \mu A$ each as well as current mirrors M_{13} - M_{14} and M_{15} - M_{16} . Current mirrors M_3 - M_4 and M_5 - M_6 drive $20 \mu A$ each. In this way, when the input signal V_{IN} equals the reference voltage V_{REF} then $I_n = I_p = I_{BiasP} - I_{biasN} = 20 \mu A$. The input unbalance gives rise to a current through resistor R_7 which value controls the slope of the V-to-I output currents. Fig. 3 shows the transfer function of three V-to-I converters connected to three different reference voltages V_{REF1} , V_{REF2} , and V_{REF3} . Notice the non-linear response with large signals and the saturation with large inputs. However, the linearity of the used region is enough for our specifications. Resistors

R_n ($n = 1, \dots, 6$) improve matching performance of current mirrors.

Figure 2. V-to-I circuit diagram.

Figure 3. Voltage-to-current transfer function of V-to-I converters.

B. Common mode feedback network

The scheme of the common mode feedback control used is shown in Fig. 4. It generates the control of the current sources used in the V-to-I scheme (Fig. 2) for compensating in the current domain for the effect of the common-mode component of the input. The obtained result is adequate for common modes as large as ± 150 mV that is 30% of the full scale.

The scheme is made by two parts: the first consists in a differential pair (transistors M_{32} and M_{33}) that measures the common mode term, V_{CM} , by the two resistors, R_1 and R_2 , nominally equal.

Figure 4. Schematic diagram of common mode feedback block.

The second part is a V-to-I, whose inputs are V_{CM} and the desired value (i.e. the analog ground A_{GND} shifted down by n-channel gate-to-source voltage). The outputs of this scheme are the gate biasing voltages V_{CMFPj} ($j = 1, \dots, 4$) and V_{CMFNm} ($m = 1, \dots, 4$) required by the current sources of the V-to-I scheme.

C. Latch interpolator

The use of the I-to-V of Fig. 1, and the successive transformation to voltage replaces in a power effective way the pre-amplifier that is normally used before the latch when the LSB is less than 40-60 mV. The latch uses a double positive feedback made by the pairs M_2 and M_3 and M_5 and M_6 . The transistors M_1 and M_4 ensure the reset. Notice that the separation of the regenerative loop and the input pair M_9 and M_{10} as required during the reset is normally realized with transistors in between the two loops [5]. However, the solution generates a large sensitivity to the threshold mismatch of the pair used for the separation, as the mismatch would modulate drain-to-source voltages that are sensitive for turning on a regenerative loop. Moving the pair in the position of M_6 and M_7 , as shown in Fig. 5 significantly reduces the sensitivity and gives rise to excellent Monte Carlo results. Obviously M_7 and M_8 , turning off the circuit in the reset clock period, benefit the dynamic current consumption.

The simulated single latch current consumption is approximately 20 μA , considering a power supply voltage equal to 0.9 V and a working frequency equal to 100 MHz. As mentioned above, in the proposed converter architecture an interpolation factor of 4 is required. The interpolation is implemented directly in the latch input transistors, as shown in Fig. 6. Indeed, by choosing an adequate number of gates

making the input transistors, it is possible to drive them using two inputs, thus achieving interpolation.

Figure 5. Latch structure.

In our case we use 4 fingers and N are connected to one inputs and $(4 - N)$ to the other input. Therefore the output of the latch is high when

$$\frac{N-1}{N} I_{n_{p1}} + \frac{1}{N} I_{n_{p2}} > \frac{N-1}{N} I_{n_{n1}} + \frac{1}{N} I_{n_{n2}} \quad (1)$$

where $I_{n_{p1}}$ and $I_{n_{p2}}$ are the positive differential input signals, while $I_{n_{n1}}$ and $I_{n_{n2}}$ are the negative ones. The aspect ratio of each finger is 2/0.26 for limiting the threshold mismatch and ensuring a good INL and DNL in the worst technological case.

Figure 6. Latch interpolator scheme.

Figure 7. Simulated differential non-linearity response.

Figure 8. Simulated integral non-linearity response.

IV. SIMULATION RESULTS

The proposed flash ADC has been simulated at transistor level by using a 0.18- μm CMOS technology. The converter has been evaluated in terms of differential non-linearity

(Fig. 7) and integral non-linearity (Fig. 8). Simulation results show that both DNL and INL are less than 0.25 LSB.

The output spectrum has been evaluated by considering different input frequency signals, f_{IN} , and a clock frequency equal to 100 MHz. Simulation results show a tone free noise floor at -60 dB, made by 2048-points FFT and $f_{IN} \approx 20$ MHz. Fig. 9 shows the output spectrum at Nyquist, 50 MHz. Under these conditions, the noise floor level increases. However, the obtained signal-to-noise ratio is 40 dB, which corresponds to 5.9 bit of resolution. It can be further noted that replica of the third and the fifth harmonics appear. The achieved SFDR is about 40 dB. The simulated total power consumption is 4.6 mW.

Figure 9. Simulated output spectrum at Nyquist.

V. CONCLUSION

In this paper the design of a low-power 6-bit flash A/D converter has been presented. The desired resolution has been achieved by using the voltage-to-current conversion strategy. The sampling frequency is 100 MHz and the proposed converter is able to work with an input signal frequency very close to Nyquist rate. The achieved figure of merit is equal to 0.75 pJ/conv and the simulated INL and DNL are both less than 0.25 LSB.

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