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A Voltage-to-Pulse Converter for Very High Frequency DC-DC Converters

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Abstract – This work presents a new control circuit that uses a voltage-to-time converter to realize high switching frequency DC-DC converters. The proposed solution is adopted in a 20-MHz DC-DC buck converter. Simulation results demonstrate the effectiveness of the approach showing very fast load and line-regulation transient responses (around 1.5 μ s) when using a 250-nH inductor and a 10- μ F output capacitor. The simulated peak power efficiency is 90%.

I. INTRODUCTION

The fast market growth of battery-operated portable applications such as digital cameras, personal digital assistants, cellular phones, MP3 players, medical diagnosis systems, etc. demands for more and more efficient power management systems. In this area, DC-DC converters, [1], play a critical role in keeping long battery life while still providing stable supply voltage together with the required driving capability. Key features of DC-DC converters are small size, low cost together with faster load and line-regulation transient responses and high power efficiency. Recently, in portable applications, a widely adopted strategy to reduce power consumption consists in using multiple supply voltages for different functional blocks so that a number of DC-DC converters has to be used. In order to reduce the overall area occupation there are two possibilities. On one hand the use of single-inductor multiple outputs DC-DC converters, [2], [3], and, on the other hand, the use of high switching frequency. Indeed, the increase of the latter in a DC-DC converter allows smaller external components (inductor and output capacitor) to be used and faster load and line-regulation transient responses. With conventional CMOS technologies (e.g. 0.5- μ m gate length) and plain PWM control solutions, it is difficult to realize regulators with a switching frequency higher than 3-5 MHz. This is mainly due to the operational amplifiers and comparators design issues, specially regarding power consumption and bandwidth.

This work presents a new DC-DC control circuit, which uses a voltage-to-time converter to realize an high switching frequency DC-DC buck converter. The proposed solution replaces the conventional PWM control blocks with a voltage-to-time converter, thus avoiding the use of operational amplifiers, voltage comparators and saw-tooth generators and allowing very high switching frequency. The proposed circuit has been used in a DC-DC buck converter and simulated by using

a conventional 0.5- μ m CMOS technology. Under these conditions, the switching frequency is 20 MHz, but the use of a 0.18- μ m CMOS technology allows higher switching frequencies (up to 100 MHz). It is worth to point out that the proposed control circuit can be employed as basic block also for other DC-DC converter topologies control strategies. Simulation results at transistor level demonstrate the effectiveness of the approach showing very fast load and line-regulation transient responses (around 1.5 μ s) together with a peak of power efficiency as high as 90% when using a 250-nH inductor and a 10- μ F output capacitor.

II. CIRCUIT DESCRIPTION

Fig. 1 shows the block diagram of the proposed DC-DC switching converter. The voltage-to-time (V2T) converter, controlled by a master clock, in the control feedback loop processes the error ($\epsilon = V_{set} - V_{out}$) and, through a driver stage (DRVR), manages the switching DC-DC converter.

Fig. 1. High frequency DC-DC switching converter block diagram.

Fig. 2 shows the conceptual scheme of the V2T converter. The basic idea is to obtain a variable delay between the rising edge of the input clock signal and the rising edge of the output pulse, which depends on the applied input voltage, V_{in} .

When the clock signal is low, the p -channel transistor MP_1 is turned on, the capacitor CPN is discharged, the voltage $V_{c,bot}$ is equal to the supply voltage and the output voltage is low. When the clock signal rises up, MP_1 is switched off, the n -channel transistor MN_1 is on

When the voltage $V_{c,bot}$ becomes lower than the threshold voltage (V_{TH}) of the

Fig. 2. V2T converter conceptual scheme.

inverter pair MP₂-MN₂, the output voltage goes to the high logic level. The delay between the rising edge of the clock signal and the rising edge of the output voltage can be expressed as follows:

$$t_{pulse} \approx R_S \cdot CPN \cdot \frac{V_{supply} - V_{TH}}{V_{in} - V_{th,MN1}} \quad (2)$$

The product (R_S -CPN) determines the gain of the circuit. It is worth to point out that the V2T converter does not require any quiescent current, thus increasing the power efficiency performance.

Fig. 3 shows a detailed schematic diagram of the V2T converter. The first two inverter stages, MP_2 - MN_2 and MP_3 - MN_3 need shoot-through current protection in order to minimize the overall circuit power consumption. It has to be underlined that it is better to implement capacitor CPN in n-well in order to minimize the noise coupling between the power stages and the V2T converter. Finally, the value of R_S can be foreseen programmable in order to obtain the desired circuit gain. As mentioned above, a buck converter topology has been chosen to validate the control strategy. Fig. 4 shows the used DC-DC buck converter architecture. The product $(R_S \cdot CPN) \cdot R_S \cdot CPN_{set}$ the loop gain and the ESR of the output capacitor C achieves the loop compensation. A switched-capacitor logic processes the voltage error $\varepsilon = (V_{ref} - V_{out})$ and drives the Voltage-to-Time converter. A conventional driver structure with automatic dead-time control drives the two MOS power transistors gates. Transistors MP and MN sizes have been chosen to correctly drive a maximum output current of 1 A.

Separate power and ground pads have been provided in order to minimize the commutation noise issues due to the parasitic bonding inductances.

Fig. 3. Voltage-to-Time converter detailed schematic diagram.

Fig. 4. Used DC-DC buck converter architecture.

III. SIMULATION RESULTS

The proposed circuit has been fully implemented at transistor level and simulated in a conventional 0.5- μm CMOS technology, allowing a switching frequency of 20 MHz. It is worth to point out that the proposed control circuit has been simulated also using a 0.18- μm CMOS technology showing that frequency as high as 100 MHz can be reached.

Fig 5. Load-regulation simulation ($L = 0.5 \mu\text{H}$, $C = 4.7 \mu\text{F}$).

Several load regulation simulations have been performed. For all these simulations, the supply voltage is 3.6 V and the output current has a step-change of 1 A. Two

different values of the inductor and of the output capacitor have been simulated.

Fig. 5 shows the load transient with an inductor of 500 nH and an output capacitor of 4.7 μ F. The positive and negative output voltage overshoots due to the ESR are about 100 mV and the settling time is about 3 μ s. A shorter settling time (about 1.5 μ s) can be obtained by using an inductor of 250 nH and an output capacitor of 10 μ F. Fig. 6 shows the load transient under these conditions. The positive and negative output voltage overshoots due to the ESR are again about 100 mV.

Fig 6. Load-regulation simulation ($L = 0.25 \mu\text{H}$, $C = 10 \mu\text{F}$).

For line regulation simulations, the used inductor and output capacitor are equal to 250 nH and 10 μ F, respectively. The nominal supply voltage is 3.6 V and the switching frequency is 20 MHz. The used input capacitor is 10 μ F. Fig. 7 shows the line transient for a step-up variation of the supply voltage of 10%. It can be noted that the voltage increase is about 30 mV. Fig. 8 depicts the line transient with a step-down variation of the supply voltage of 10%. It can be noted that the voltage drop is again about 30 mV.

Fig. 7. Line-regulation simulation ($L = 0.25 \mu\text{H}$, $C_{\text{out}} = 10 \mu\text{F}$, $C_{\text{in}} = 10 \mu\text{F}$, +10% input voltage variation).

Fig. 9 shows the simulated power efficiency as a function of the output current, when using a supply voltage equal to 3.6 V and considering real power switches (transistors size reported in Fig. 4). The regulated output voltage is 1.8 V. It can be noted that the peak efficiency is equal to 90.1% for an output current equal to 500 mA. For low currents (100 mA) the power efficiency drops, but it is always higher than 83%.

Fig. 8. Line-regulation simulation ($L = 0.25 \mu\text{H}$, $C_{\text{out}} = 10 \mu\text{F}$, $C_{\text{in}} = 10 \mu\text{F}$, -10% input voltage variation).

Fig 9. Simulated power efficiency as a function of the output current ($L = 0.25 \mu\text{H}$, $C = 10 \mu\text{F}$).

CONCLUSIONS

In this paper a new control circuit for very high frequency DC-DC converters has been proposed. The control strategy is based on a Voltage-to-Time converter. The proposed circuit has been implemented and simulated in a 20-MHz DC-DC buck converter by using a conventional 0.5- μ m CMOS technology. In scaled technology, the proposed circuit allows achieving DC-DC converters working at very high frequency (e.g., 100 MHz with a 0.18- μ m CMOS technology). Simulation results show very fast load and line-regulation transient responses (around 1.5 μ s) with an inductance of 250 nH and an output capacitor equal to 10 μ F. The simulated peak of power efficiency is equal to 90%.

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