M. Casubolo, M. Grassi, A. Lombardi, F. Maloberti, P. Malcovati: "**A Two-Bit-per-Cycle Successive-Approximation ADC with Background Offset Calibration**"; 15th IEEE Int. Conf. on Electronics, Circuits and Systems, ICECS 2008, St. Julien's, August 31-September 3, 2008, pp. 650-653.

©20xx IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

A Two-Bit-per-Cycle Successive-Approximation ADC with Background Offset Calibration

Michele Casubolo¹, Marco Grassi¹, Andrea Lombardi¹, Franco Maloberti², and Piero Malcovati¹

¹Department of Electrical Engineering and ²Department of Electronics

University of Pavia, Pavia, Italy

Email: michele.casubolo@fastwebnet.it, {marco.grassi, andrea.lombardi, franco.maloberti, piero.malcovati}@unipv.it

Abstract—In this paper we present a 10-bit, two-bit per cycles successive-approximation A/D converter (ADC). The circuit, operated at 60 MHz clock frequency, achieves a sampling frequency of 10 MHz, requiring only 6 clock cycles to accomplish a conversion. The ADC exploits three comparators to resolve two bits during each conversion cycle. To avoid the severe performance degradation due to offset mismatches among the comparators, we developed a novel background offset calibration technique. During the input signal sampling phase, when the comparators would otherwise be idle, we reconfigure the circuit to implement three one-bit per cycle, 8-bit successive-approximation ADCs, which within 8 conversion cycles measure the offset of each comparator. The effect of the comparator offset is then canceled in the digital domain. Simulation results confirm the effectiveness of the proposed solution, allowing to achieve 10 bits of resolutions even in the presence of large offsets in the comparators.

I. INTRODUCTION

The prerequisite of Moore's law is the continued down-scaling of CMOS technology, which produces yet faster and more power-efficient digital circuitry. However, most technology parameters important for analog design suffer degradation in scaled technologies. As the minimum feature size decreases, so does the gate oxide thickness, causing still lower allowable supply voltages. The present state-of-the-art 65 nm technology node features a maximum supply voltage of only 1 V for the standard MOS transistors. This supply is expected to decrease to 0.7 V for the upcoming 45 nm node projected in 2009 [1]. As the device threshold voltages do not scale proportionally with decreasing supply voltage, the available voltage swing decreases which effectively disallows the use of stacked MOS circuit configurations. A common measure of technology speed is the device transition frequency f_T [2], which increases with each new technology node, thus increasing the bandwidth of analog circuits. Furthermore, the availability of still better lithography processes, enhances the absolute matching of on-chip components for a fixed area [1]. Unfortunately, decreasing the feature size also decreases the Early voltage V_A and hence the device output resistance r_o . Decreasing channel resistivity leads to decreasing intrinsic DC gain ($A_0 = g_m r_o$), thus reducing the inherent circuit accuracy [2]–[4].

In the design of A/D converters (ADCs) with a bandwidth in the MHz range, the increase of MOS transistor response speed in scaled technologies allows the designer to consider topologies typically used only for low-frequency applications.

Fig. 1. Simplified block diagram of the successive-approximation (SAR) ADC

However, reduced analog performance, especially in terms of gain, may be reflected in increased power consumption for a desired ADC accuracy, as circuit complexity increases to compensate for intrinsic technology shortcomings. For this reason, a key feature of low-power ADCs in deep sub-micron technologies would be to use topologies that do not rely on high-gain feedback loops for successful operation. Further, the improved matching of passive devices in ever down-scaled technologies favors ADC topologies that are based on passive device matching. In view of these considerations the successive-approximation (SAR) topology appears to be an excellent candidate for implementing power-efficient ADCs with resolution of the order of 8-12 bits and bandwidth in the MHz range [5]–[11].

II. SUCCESSIVE-APPROXIMATION ADCs

The simplified block diagram of a SAR ADC [12] is shown in Fig. 1. The circuit, consisting of a sample-and-hold (S/H), a comparator (CMP), a D/A converter (DAC) and a digital successive-approximation register (SAR), does not require any high-performance active analog block, besides just one comparator, and the accuracy of the A/D conversion is basically determined by the accuracy of the DAC.

A conventional SAR ADC requires $N + 1$ clock cycles for achieving an N -bit A/D conversion: one clock cycle for sampling the input signal and N clock cycles for accomplishing the successive-approximation algorithm. Therefore, assuming a clock frequency f_{ck} , the maximum achievable sampling frequency is $f_s = f_{ck} / (N + 1)$, while, for example, a pipeline or a flash ADC achieves $f_s = f_{ck}$, but at the expense of a larger number of active analog components, which are critical in scaled CMOS technologies and require large power consumption. SAR ADCs are, indeed, extremely power efficient. If we consider the figure of merit

$$FoM = \frac{P}{2 \cdot B \cdot 2^{ENOB}}, \quad (1)$$

where P is the power consumption, B the bandwidth ($B = f_s/2$ for Nyquist rate ADCs) and $ENOB$ the effective number of bits, all of the ADCs presented in literature, with $FoM \leq 100$ fJ/Conversion-step are based on the SAR architecture (for example, the ADC presented in [7] achieves the record FoM value of 4.4 pJ/Conversion-step).

However, for high-speed ADCs, when the required sampling frequency is such that the clock frequency approaches the maximum value allowed for a given technology, the number of clock cycles required for achieving a conversion becomes a severe limitation for the exploitation of the SAR ADC power efficiency and other less power efficient topologies have to be used. There are two possible solutions, both based on parallelism, for overcoming this limitation, namely using time-interleaved structures or increasing the number of bits resolved in each cycle by the SAR topology.

The time interleaved solution has been successfully used for implementing high-speed SAR ADCs [6], [13]. However, offset, gain and timing mismatches among the time-interleaved paths are strongly degrading the performance of the ADC for resolutions higher than 5-6 bits, unless some sort of calibration is used. Moreover, the area penalty of this solution is substantial, since M equal ADCs are used to increase the sampling frequency by a factor M (without considering eventual calibration circuits).

The other possible solution for increasing the sampling frequency of a SAR ADC for a given clock frequency is to resolve $M > 1$ bits in each conversion cycle [14]. This solution requires the use of 2^M comparators, which operate in parallel. The area penalty, in this case, is limited, while the sampling frequency becomes $f_s = f_{ck}/(N/M + 1)$. However, the offset of the comparators, which for conventional SAR architectures is negligible, becomes an issue. Indeed, while in standard SAR topologies the offset of the comparator leads to a corresponding offset of the ADC (which is usually not important), when M bits are resolved in each cycle, offset mismatches among the 2^M comparators lead to non-linearity (i.e. to degradation of INL , DNL , $SNDR$ and $SFDR$). Therefore, in order to use this solution we have either to overdesign the comparators for reducing the offset, at the expense of power consumption, or introduce some sort of calibration. Indeed, the redundancy approach, typically used in pipeline or algorithmic ADCs, is not effective in this case, since no amplification takes place between one cycle and the next and the signal amplitude at the input of the comparators tends to the least significant bit (LSB) value (i.e. the mismatch among the offset of the comparators has to be lower than half of the LSB).

In this paper we propose a SAR ADC which resolves two bits per cycle (i.e. requires 6 clock cycles to achieve 10 bits of resolution) and uses a background calibration scheme in the digital domain to compensate the comparator offset mismatch. This solution allows us to achieve a significant improvement of the sampling frequency for a given clock frequency, with limited area and power consumption penalties. Moreover, since offset calibration is performed in the digital domain, we can take full advantage of scaled CMOS technologies.

Fig. 2. Block diagram of the proposed 10-bit, two-bit per cycle SAR ADC

Fig. 3. Operating principle of the two-bit per cycle SAR ADC

III. TWO-BIT PER CYCLE SUCCESSIVE-APPROXIMATION ADC

The block diagram of the proposed 10-bit, two-bit per cycle SAR ADC is shown in Fig. 2. The circuit consists of a passive sample-and-hold block (S/H), three latched comparators, a resistive-string based DAC with three multiplexers (MUX) and a digital block implementing the successive-approximation register (SAR) and the offset compensation algorithm.

The ADC requires 6 clock cycles to accomplish the 10-bit A/D conversion. The first clock cycle ($T_{S/H} = T_{ck}$) is used for sampling the input signal, while the remaining 5 clock cycles ($T_C = 5 \cdot T_{ck}$) are used to perform the A/D conversion. Assuming that the input signal has been sampled during $T_{S/H}$, during each of the 5 clock cycles of T_C , the ADC determines in which part α of the selected range lies the input sample (the selected range is divided in four parts by the three comparators and only one is selected). In the first cycle of T_C the selected range is the full input signal swing, while in the next cycles it is equal to α (as determined in the previous cycle). Fig. 3 shows a simple example with only six bits. The colored area in Fig. 3 denotes the analog value corresponding to the bits already determined. The SAR stores the bits already resolved and drives the three multiplexers to provide the proper reference voltage to each comparator in each cycle, as in conventional successive-approximation ADCs.

The schematic of a typical comparator used in SAR ADCs is shown in Fig. 4. The circuit consists of a gain stage (M_1 , M_2), a double latch (M_3 , M_9 and M_4 , M_{10}) and a set-reset

Fig. 4. Schematic of a typical comparator used in SAR ADCs

flip-flop. The offset of this comparator is dominated by the threshold voltage mismatch of transistors M_1 and M_2 , which is inversely proportional to $\sqrt{W \cdot L}$, W and L denoting width and length of the transistors, respectively. As already mentioned, offset mismatches among the three comparators lead to non-linearity in the A/D conversion. Therefore, in order keep the offset low, the area of M_1 and M_2 has to be designed very large. This, however, strongly increases the parasitic capacitances, thus reducing the f_T of the transistors and hence the maximum clock frequency of the ADC. As a result, we loose the speed improvement obtained by resolving two bits per clock cycle.

To overcome this problem, the only viable solution is offset calibration, which allow the comparator offset mismatch to be canceled without increasing the transistor area. The basic idea behind the offset calibration technique used in the proposed ADC stems from the observation that during the sample time $T_{S/H}$ the comparators are idle. Therefore, we can use this time period to measure the offset of the comparators, which can then be corrected in the digital domain. The offset measurement is performed by connecting the signal inputs of the comparators to analog ground and reconfiguring the ADC in order to realize three one-bit per cycle SAR ADCs, which convert the offset in the digital domain. Since only one clock period is available in each conversion cycle to carry out the offset measurement, the successive-approximation algorithm has to be split across more conversion cycles. In the proposed ADC we perform the offset measurement with 8-bit resolution. Therefore, the correct offset value is available in the digital domain after 8 conversion cycles and it is periodically updated, thus allowing offset variations due to temperature or ageing to be tracked. The measured offset values are then added in the digital domain to the word representing the reference voltage provided by the SAR to the each comparator, thus actually canceling the offset. In order to avoid overflow in the reference voltage generation, we added a few over-range levels in the DAC (1278 instead of 1024 levels, as shown in Fig. 2). A timing diagram of the operations carried-out during the A/D conversion is shown in Fig. 5. The proposed offset calibration technique is working in background and it is not affecting the normal operation of the ADC.

The block diagram of the digital circuit implementing the above mentioned functions is shown in Fig. 6. The block

Fig. 5. Timing diagram of the operations carried-out during the A/D conversion

Control Logic is in charge of controlling the sequence of operations, while the *Decoder* block transforms the binary output of the *Adder* into suitable signals for driving the multiplexers of the DAC. The *Offset Compensation Register* and the *SAR* blocks implement the successive-approximation algorithms for the conversion of the offset and of the input signal, respectively.

IV. SIMULATION RESULTS

The proposed ADC has been extensively simulated with MATLAB/SIMULINK. The circuit is operated with a clock frequency $f_{ck} = 60$ MHz and hence a sampling frequency $f_s = 10$ MHz. The digital section has been implemented in VHDL. In order to verify the effectiveness of the proposed solution we simulated the static integral (*INL*) and differential (*DNL*) non-linearities with and without offset calibration, in the presence of an offset as large as 32 times the least-significant bit (LSB). The results, reported in Fig. 7 and Fig. 8, confirm that the proposed background offset calibration technique allows a 2-bit per cycle SAR ADC to be implemented without performance penalty. Fig. 9 shows the spectrum of the ADC output, obtained applying a 1 MHz full-scale sinusoidal input signal, with and without offset calibration. The significant harmonic distortion in the spectrum due to the offset mismatches among comparators disappears when offset calibration is turned on. The ADC achieves a signal-to-noise-and-distortion ratio (*SNDR*) of 34 dB (5.35 bits of resolution) without offset calibration and 62 dB (10 bits of resolution) with offset calibration. Obviously, when considering also thermal noise and mismatches in the DAC the achieved *SNDR* could be slightly degraded.

V. CONCLUSIONS

In this paper we proposed a two-bit per cycle SAR ADC, which requires only 6 clock cycles to achieve 10 bits of resolution. The circuit, operated with a clock frequency of 60 MHz, achieves an effective sampling frequency of 10 MHz. Thanks to a novel background offset calibration technique, the performance of the ADC is not degraded even in the presence of 32-LSB comparator offset mismatch. Simulation results confirmed the validity of the proposed solution.

Fig. 6. Block diagram of the digital section of the proposed ADC

Fig. 7. *INL* and *DNL* of the proposed ADC without offset calibration

Fig. 9. Spectrum of the ADC output with and without offset calibration

Fig. 8. *INL* and *DNL* of the proposed ADC with offset calibration

REFERENCES

- [1] (2007) International roadmap for semiconductors (ITRS). [Online]. Available: <http://www.itrs.net>
- [2] P. Woerlee, *et al.*, “RF-CMOS performance trends,” *IEEE Trans. Electron Devices*, vol. 48, pp. 1776–1782, Aug. 2001.
- [3] V. Kilchytska, *et al.*, “Influence of device engineering on the analog and RF performances of SOI MOSFETs,” *IEEE Trans. Electron Devices*, vol. 50, pp. 577–588, Mar. 2003.
- [4] J. Pekarik, *et al.*, “RFCMOS technology from 0.25 μ m to 65nm: The state of the art,” in *Proc. IEEE CICC*, May 2004, pp. 217–224.
- [5] digital conversion techniques – part I,” *IEEE J. Solid-State Circuits*, vol. 108, pp. 371–379, Dec. 1975.
- [13] B. P. Ginsburg and A. P. Chandrakasan, “Highly interleaved 5b 250MS/s ADC with redundant channels in 65nm CMOS,” in *IEEE ISSCC Dig. Tech. Pap.*, Feb. 2008, pp. 240–241.
- [14] Z. Cao, S. Yan, and Y. Li, “A 32mW 1.25GS/s 6b 2b/Step SAR ADC in 0.13 μ m CMOS,” in *IEEE ISSCC Dig. Tech. Pap.*, Feb. 2008, pp. 542–543.