A. Agnes, F. Maloberti: "**Multi-bit High-order Incremental Converters with Digital Calibration**"; European Conf. on Circuit Theory and Design, ECCTD 2009, Antalya, 23-27 August 2009, pp. 739-742.

©20xx IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

Multi-bit High-order Incremental Converters with Digital Calibration

Andrea Agnes, and Franco Maloberti

Department of Electronics, University of Pavia

via Ferrata, 1, 27100 Pavia, Italy

Email: andrea.agnes@unipv.it, franco.maloberti@unipv.it

Abstract— Cascade scheme of single order incremental modulators that obtain high-order architectures are studied. The use of high-order obtains a high number of bit with a small number of clock periods. Moreover, it is possible to use multi-bit modulators in the last stages of the chain. The requests of low gain error in the first stages of the cascade are satisfied with an off-line gain mismatch error and digital calibration of result.

I. INTRODUCTION

Incremental converters can be viewed as an extension of the ramp converter. In the ramp scheme the input voltage is accumulated a given number of times to produce a step-up ramp and than the result is measured using the reference voltage which has the purpose to obtain a step-down ramp for a suitable number of clock cycles. In the incremental architecture the feedback path, which provides negative steps equal to the reference at the input, interleaves the rising ramp with falling ramp [1]. This is what happens in a first order incremental modulator. The second order one is realized with the cascade of two integrators that generate a rising parabola. In this case, the feedback paths interleaves the parabola and injects the obtained signal to the input of the first and the second stage [2]-[3].

Incremental schemes use two levels DACs because multi-bits solutions require very high linearity, difficult to obtain. Moreover, dynamic matching techniques are not suitable because incremental converter does not exploits features in the frequency domain but, even if “oversampled”, is a Nyquist rate solution.

The swing of the used integrators in incremental schemes can be many times the reference when input is near the boundary limits, especially for second order schemes, as discussed in the next section. Result is that for a given op-amp dynamic range the input must be a fraction of it, and this reduces the SNR when the kT/C noise is a limit.

This paper proposes a high order incremental scheme made by the cascade of single order incremental converters. It is shown that the cascade of 5 stages obtains a resolution of 19 bit of accuracy, with 2 and 3 bit resolution in the two last stages and 32 clock periods for conversion. The limit is caused by mismatch in the gain of cascaded stages which is compensated by digital calibration. Simulation results demonstrate the validity of the method and quantify the required accuracy in the calibration network.

II. CONVENTIONAL INCREMENTAL CONVERTERS

Fig. 1 shows the architecture of a first and second order incremental scheme. Assuming that input is constant for the entire conversion period, the analog signal at the output of the integrator is

$$R_1(k) = \sum_{i=1}^k X_{in}(i) - \sum_{i=1}^k Y_1(i) \quad (1)$$

$$R_2(k) = \sum_{i=1}^k \sum_{j=1}^i X_{in}(j) - \sum_{i=1}^k \sum_{j=1}^i Y_2(j) - \sum_{i=1}^k Y_2(i) \quad (2)$$

for a first and second order scheme respectively. k is a generic clock period after beginning conversion. At the end of the conversion, $k = N$, the values of residuals $R_1(N)$ or $R_2(N)$ are neglected and (1) and (2) are used to measure X_{in} . The full scales are N and $N(N+1)/2$ respectively. The errors of measures are

$$\epsilon_1 = \frac{R_1(N)}{N}; \quad \epsilon_2 = \frac{R_2(N)}{\frac{N \cdot (N+1)}{2}} \quad (3)$$

therefore, supposing $R_1(N)$ and $R_2(N)$ negligible with respect to the terms on the right sides, the obtained solutions are

$$bit_1 = \log_2(N); \quad bit_2 = \log_2(N \cdot (N+1)/2) \quad (4)$$

for the first and the second order respectively.

The amplitude of analog internal nodes of the first and second order modulators are limited when the DC input in well inside the $(-1/2V_{ref}, \dots, +1/2V_{ref})$ range, typically,

Fig. 1. First order and Second order Incremental Converter.

with a module that is less than $2V_{ref}$. However, when the input approaches the boundary limits the analog amplitudes becomes very large, especially for the second order scheme, because of a weakened loop control.

III. CASCADE OF FIRST ORDER INCREMENTAL BLOCKS

The analog swing in a modulator with reference $\pm V_{ref}$ and input $(1/2 \cdot V_{ref} - \delta)$ (δ a small quantity) is, as shown in Fig. 2, 50% wider than reference for the first order modulator (a) but almost two times the reference for the first integrator (b) and three times for the second integrator (c) in a second order scheme. Therefore, with equal dynamic ranges it is necessary to use a bigger attenuation at input of a second order modulator or to use an attenuation factor between first and second integrator. Both solutions cost extra resolution.

A more effective architecture is a MASH-like cascade of two first order schemes. The use of two local feedback improves the controls of the op-amp swing with a peak amplitude of the second op-amp equal to about twice the reference [4].

The above considerations are the basis of the proposed architectures: a cascade of first order schemes with a proper interstage attenuation that keeps limited the op-amp swings. The cascade of 4 integrators obtains, after N clock periods, a full scale input amplification equal to

$$A_{FS} = a_1 a_2 a_3 \frac{N(N+1)(N+2)(N+3)}{4!}; \quad (5)$$

and, with a cascade of 5 integrators, it results

$$A_{FS} = a_1 a_2 a_3 a_4 \frac{N(N+1)(N+2)(N+3)(N+4)}{5!}; \quad (6)$$

and so forth. Accordingly, the cascade of two integrators with $a_1 = 1/2$ needs $N = 1448$ to obtain 19 bit. A fourth order with

Fig. 2. Analog output swing in a first order modulator (a) and each integrator in a second order modulator (b-c).

Fig. 3. $\Sigma\Delta$ Mash converter with 5 modulators.

$a_1 = a_2 = a_3 = 1/2$ needs 99 clock periods and a fifth order requires 62 clock periods.

Fig. 3 illustrates the cascade of five first order modulators. The input of each modulator is the residual of the previous one and not the quantization error as it is done in $\Sigma\Delta$ MASH converters. The reason of the choice is that the amplitude of residual is almost equal to the quantization error and it does not make sense to perform subtractions that likely, introduces an extra error. The sum blocks used in each modulator obtains

$$Out(k) = \sum_{i=1}^k In(i) = \mathcal{I}_k(In) \quad (7)$$

that defines the operator $\mathcal{I}$, discrete-time accumulator in the time domain. By inspection of the scheme of Fig. 3, after N clock periods, it results

$$R_1(N) = \mathcal{I}_N(X_{in}) - \mathcal{I}_{N-1}(D_1), \quad (8)$$

$$R_2(N) = a_1 [\mathcal{I}_N(\mathcal{I}_N(X_{in})) - \mathcal{I}_N(\mathcal{I}_{N-1}(D_1))] - \mathcal{I}_{N-1}(D_2), \quad (9)$$

....

$$R_5(N) = a_1 a_2 a_3 a_4 \{ \mathcal{I}_N [\mathcal{I}_N [\mathcal{I}_N [\mathcal{I}_N [\mathcal{I}_N (X_{in})]]]] \} - a_1 a_2 a_3 a_4 \{ \mathcal{I}_N [\mathcal{I}_N [\mathcal{I}_N [\mathcal{I}_N [\mathcal{I}_{N-1}(Y_1)]]]] \} - a_2 a_3 a_4 \{ \mathcal{I}_N [\mathcal{I}_N [\mathcal{I}_{N-1}(Y_2)]] \} - a_3 a_4 \{ \mathcal{I}_N [\mathcal{I}_{N-1}(Y_3)] \} - a_4 \{ \mathcal{I}_{N-1}(Y_4) \} - \mathcal{I}_{N-1}(Y_5) \} \quad (10)$$

showing that the amplification of the input is by a factor obtained by the first term. The amplified input is approximated by a suitable digital processing of five digital outputs.

Equation (10) shows that the digital processing performs a weighted superposition of the various bitstreams with a weight that increase at early occurrences. A bit that is 1 at the last clock cycle has weight 1 for all modulators. A bit that is 1 ten clock periods before the end of conversion is multiplied

Fig. 4. Proposed high order Incremental architecture.

by 10, 55, 220 and 715 for the second, third, fourth or fifth modulator respectively. A bit that is 1 eleven clock period before is multiplied by 11, 66, 286 and 1001 respectively. The increases equal the multiplication factor of the previous quantizer on the same clock period (i.e. $1001 = 715 + 286$).

In order to reduce the conversion time, the last modulators of the cascade can use multi-bit quantizers. In this case the input of next modulator is the quantization error instead than the residual because is smaller. The attenuation factor is not necessary anymore and, eventually, can become a gain. The above leads to a variety of architectures. The one used in this paper as study case is shown in Fig. 4. It uses the cascade of three first order modulator with a single comparator and interstage attenuation $1/2$ followed by two stages one with 2 and the other with 3 bit and no interstage attenuation. The scheme obtains an overall expected resolution of more than 19 bit with $N = 32$.

IV. IMPLEMENTATION ISSUES

The implementation and the choice of architectures made by the cascade of incremental converters depends on the following issues:

- the possible gain error, that can be caused by mismatches, must be smaller than the smallest signal which introduces a correction of a LSB by the successive blocks;
- the linearity of a multi-bit DAC must be better than the accuracy from the considered modulator (included) to the end of the chain;
- the dynamic range at the input of each modulator must be such to keep the analog swing of the used op-amp;

The worst case for gain mismatch is when input of a modulator is, in average, at half range. If the input is constant across the midrange the output is a sequence of 1 and 0 with first bit 1 if $X_{in} = +\delta$ and first bit 0 if $X_{in} = -\delta$. The difference between these two sequences, after a cascade of integrators, gives a quantity Δ_{Tr} , that must be compensated for bit sequences of the next stages of the cascade. However,

if residual is transferred with an error caused by mismatch, ϵ_G , there is an error in compensation equal to $\Delta_{Tr} \cdot \epsilon_G$. Therefore, the admitted gain error is proportional to the inverse of Δ_{Tr} .

The use of the cascade of G integrators for N clock periods gives the value of Δ_{Tr} listen in Table 1.

Table 1

G	Δ_{Tr}
2	$G_2 = N/2$
3	$G_3 = G_2(G_2 + 1)$
4	$G_4 = 4G_3(G_2 + 2)/6 - G_3/2$
5	$G_5 = G_4(G_2 + 2)/6 - 5G_4/8 + G_3/16$

A second order modulator made by the cascade of two first orders requires a gain error, ϵ_G , lower than $2/N$, condition easily obtainable even with large values of N . On the contrary, when G is 4 or 5, required gain accuracy is difficult to obtain, in particular in the first integrators. Therefore, as discussed shortly, it may be necessary to use digital calibration.

The linearity of a DAC possibly used in the modulator is a limit when the resolution from that modulator to the end of the cascade is high, typically larger than 10-bit. Since a cascade of a large number of stages distributes resolution among stages, depending on design, the last stage or even the last pair of stages provide 8–9 bit. Such a linearity is easily satisfied and resolution can improve.

V. COMPUTER SIMULATIONS

The architecture of Fig. 4 has been simulated at behavioral level with ideal interstage gain and ideal op-amps. Simulation results with ideal elements confirm the expected behavior. The simulated DNL is zero in the entire dynamic range. With interstage gain errors the DNL remains almost unchanged but the INL jumps at critical transitions. The input-output characteristic, of Fig. 5, underlines the effects for three different interstage gain errors between first and second stage. In particular a gain error smaller than $30ppm$ ensures the monotonic trend of the input-output characteristic. The accuracy required at three σ is provided by matching of big integrated capacitors. Suppose to use a technology that ensures matching accuracy with $\sigma = \frac{0.3\%}{\mu m^2}$. Since accuracy improves as $\frac{1}{\sqrt{A}}$, where A is the area of the plate, 30 ppm requires $10,000\mu m^2$ but if the designer want to ensure 3σ accuracy the area becomes

Fig. 5. Input vs Output characteristic around the zero, with error of a_1 equal to $3 \cdot 10^{-5}$ (a), $15 \cdot 10^{-5}$ (b) and $3 \cdot 10^{-4}$ (c).

Fig. 6. Different INL with error on first (a), second (b) or third element (c).

$90,000\mu m^2$ corresponding to about $80pF$, much more than the value required by the $\frac{kT}{C}$ limit.

The interstage error becomes less critical for the second and third gain error. Fig. 6 shows the *INL* with $N = 32$. Used errors are 0.1%. The worst case is for the first interstage. At midrange the *INL* changes by 35 *LSB*. Same gain error on the second stage causes an *INL* change by ± 1.5 *LSB*. For the last interstage error the limit is less than ± 0.5 *LSB*.

The performed behavioral simulations account for real gain and bandwidth of operational amplifiers. In a switched capacitor integrators the finite op-amp gain is such that

$$V_{out}(n+1) = V_{out,id}(n+1) + \epsilon_1 V_{out}(n) + \epsilon_2 V_{out}(n+1) \quad (11)$$

that causes a non-linear response due to different output patterns with very close input signals. The required gain is very high in first and second stage of the cascade (more than 100 *dB*) when 19 bit or more are needed. Gain requests are relaxed in the nest stages.

The finite op-amp bandwidth is responsible of a gain error given by

$$\epsilon_G = e^{\pi f_T T_{ck} \beta} \quad (12)$$

where T_{ck} is the clock period, f_T is the unity gain bandwidth and β is the feedback factor. This gain error is accounted for together with the interstage gain error.

VI. GAIN MEASUREMENT AND DIGITAL CALIBRATION

As discussed above interstage gain errors are key limits and for high resolutions it is mandatory to correct it or to monitor its contribution. If the gain error is measured, its effect can be corrected digitally. The *A/D* conversion is the multiple convolution of bit-streams, as calculated in (10). Since

$$\mathcal{I}_N(\mathcal{I}_N(\mathcal{I}_N(\mathcal{I}_N(\mathcal{I}_N(X_{in})))))) = FS(N) \cdot X_{in} \quad (13)$$

Neglecting $R_5(N)$, equation (10), with a simplified notation becomes

$$\begin{aligned} a_1 a_2 a_3 a_4 \cdot FS(N) \cdot X_{in} = & a_1 a_2 a_3 a_4 \cdot P_1(N) + \\ & + a_2 a_3 a_4 \cdot P_2(N) + \\ & + a_3 a_4 \cdot P_3(N) + \\ & + a_4 \cdot P_4(N) + P_5(N) \end{aligned} \quad (14)$$

where $P_i(N)$ are, for a given N , constant values calculated from the output bitstreams. Therefore, (14) is an equation with

5 unknown, X_{in} , and the four relative errors of coefficients a_i , ϵ_i , $i = 1, \dots, 4$.

Supposing to neglect the errors of the interstage gains a_3 and a_4 , for calibration we must determine the two coefficients $a_1 = \bar{a}_1 \cdot (1 + \epsilon_1)$, $\dots$, $a_4 = \bar{a}_4 \cdot (1 + \epsilon_4)$ and the unknown X_{in} . Therefore, we need three equations. One is (14) that can be written as

$$\begin{aligned} (1 + \epsilon_1) \cdot (1 + \epsilon_2) \cdot S_0(N) \cdot X_{in} = \\ = (1 + \epsilon_1) \cdot (1 + \epsilon_2) \cdot S_1(N) + \\ + (1 + \epsilon_2) \cdot S_2(N) + S_3(N) + S_4(N) + S_5(N) \end{aligned} \quad (15)$$

two other equations are obtained by running the converter with same input and N_1 or N_2 , clock periods. The system of three equations with unknown X_{in} , ϵ_1 and ϵ_2 that are solved digitally. The use of large values of N , N_1 and N_2 ensures good accuracy.

The above describes a method for the off-line measurement of the mismatch error. The operation can also be done on-line. Coefficients called in (15) S_i calculated every end of conversion and the ones at two time slots N_1 and N_2 ($N_1, N_2 < N$) are stores and accumulated for a large number, K conversion cycles. each accumulation makes an equation with again three unknown $\sum_{i=1}^K X_{in,i}$, ϵ_1 and ϵ_2 . The system of three equations is then solved digitally as done for the off-line method.

VII. CONCLUSION

A chain of first order incremental modulator obtains high resolution with relatively small number of clock cycles. The cascade of first order schemes is more convenient of high order architectures even for a second order case because multiple loops better control the swing at the output of integrators. The interstage error, not important for second order incremental converters, becomes a tangible limit for high order cascades. Switched capacitor schemes obtain a good control of the integrator gain if large unity capacitors are used. However, when necessary, digital measurement of mismatch and digital calibration are possible without requiring additional analog circuitry. Mismatch measure and calibration require only digital processing.

ACKNOWLEDGMENT

This work is supported by FIRB project, Italian National Program #RBAP06L4S5.

REFERENCES

- [1] J. Markus, J. Silva, and G. C. Temes, "Theory and Applications of Incremental $\Sigma\Delta$ Converters", *IEEE, Transactions on Circuits And Systems-I: Regular Papers*, vol.51, pp. 678-690, Apr 2004.
- [2] S. Kavusi, H. Kakavand, and A. El Gamal, "On Incremental Sigma-Delta Modulation With Optimal Filtering", *IEEE, Transaction on Circuits and Systems I*, TCAS-I, pp. 1004-1015, May 2006.
- [3] Z. Ye, and P. Kennedy, "Reduced Complexity MASH Delta-Sigma Modulator", *IEEE, Transaction on Circuits and Systems II*, TCAS-II, pp. 725-729, Aug 2007.
- [4] M. Belloni, C. Della Fiore, F. Maloberti, M. G. Andrade, "On the Design of Incremental $\Sigma\Delta$ Converters", *IEEE Midwest Symposium on Circuit and Systems*, pp. 1374-1377, 2007.