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Performance Enhanced Op-Amp for 65nm CMOS Technologies and Below

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Abstract—Multistage operational amplifiers suitable for nanometer-scale CMOS technologies and low-voltage applications are described. The low intrinsic gain of transistors is compensated for with cascade of single-stage amplifiers. Techniques for compensations are revisited and the optimal solution identified. An example of a novel scheme that achieves 67 dB of DC gain, 320 MHz of bandwidth and 61 degrees of phase margin is presented. The power consumption is as low as 0.24 mW with a slew rate of 84.5 V/ μ s. The CMOS technology is 65 nm; the design uses only minimum channel length transistors.

Index Terms—Amplifiers, compensation, multistage amplifiers, operational amplifiers.

I. INTRODUCTION

The op-amp is a key building block for analog processing. With old technologies and relatively high supply voltages consolidated schematics achieve high gain, wide bandwidth and good slew rate. With modern technologies, for which the channel length is as short as 65 nm or less, the design of an op-amp with good performances is problematic because of the intrinsic limitations of the transistor's analog performances.

The key factors limiting the analog performances of nanometer integrated circuits are:

- The supply voltage scales down but since the threshold voltage (V_T) is not expected to scale down with same pace, the dynamic range requirements impose using only two transistors from V_{DD} to V_{SS} in the output stage.
- The transconductance gain of transistors worsens and is weakly controlled by the bias current.
- The output conductance is poor making the value of the transistor intrinsic gain in the few tens range or less.

The above limits determine new challenges for analog designers that must be faced with new or renewed design methodologies. In this paper a multistage amplifier with enhancement of both dc gain and slew rate performances is presented. Simulation results with a 65 nm CMOS technology show that the proposed architecture achieves relatively high DC gain, fast operation and ensures stability, making the design strategy suitable for nanometer-scale CMOS circuits.

II. LOW-VOLTAGE MULTISTAGE AMPLIFIERS

Short-channel effects in sub-micron CMOS transistors cause a transconductance and output-impedance degradation and hence the intrinsic gain diminishes significantly. The simplest

Fig. 1. Dependence of the DC gain, A_V , on the bias current, I_B , of a CMOS analog inverter with n-channel input transistor.

form of gain stage, the inverter with active load, is used as test vehicle to verify the limit for a given technology. The use of a 65 nm CMOS process and various operational conditions leads to Fig. 1 which shows the dependence of the DC gain, A_V , on bias current, I_B . The aspect ratio of the input transistors goes from $W/L = 3.375 \mu m / 0.06 \mu m$ to values scaled up by a factor 2 and 4, respectively. The result shows that with the minimum length despite the large aspect ratio the gain is as low as 11 dB. Enlarging transistors increases the gain that goes up to just about 22 dB for low bias current. The trend is what expected but the values of gain are almost an order of magnitude lower than what an inverter with active load achieves with mature technologies.

The above result outlines the need of cascading many stages for getting a relatively large gain and this, certainly, makes more difficult ensuring stability. In addition, the low supply voltage imposed by technology makes it difficult using cascode schemes and certainly does not allow their use in the output stage. For a target gain of about 60 dB cascading three amplification stages or even more is therefore necessary [1].

A key design issue for multistage amplifiers is the closed-loop stability. Having many stages means having multiple poles at frequencies that depend on the time constant at the output node of each gain stage. The addition of the phase shift quickly goes to 180° well before the 0 dB crossing of the Bode diagram. There are various frequency-compensation

Fig. 2. Multistage frequency-compensation amplifier topologies. (a) NMC. (b) MNMC. (c) NGCC. (d) NMCNR. (e) DFCFC.

techniques, all of them based on pole-splitting or zero-pole compensation. We recall the most relevant with a three stages amplifier because three stages are the optimum trade-off between DC gain, bandwidth and consumed power for many practical circuit implementations. Fig. 2(a) illustrates the *Nested Miller Compensation* (NMC) method [2]: for the third gain stage added there is an additional Miller capacitor to give rise to a further pole splitting action. The *Multipath Nested Miller Compensation* (MNMC) [3] of Fig. 2(b) uses a feedforward path realized by a transconductance stage, G_{mf} , that bypasses the first two gain stages. The parallel action of the direct path and the feedforward path together with a proper design ensures the required stability. An improved version of the MNMC topology is the *Nested Transconductance (G_m)-Capacitance Compensation* (NGCC) [4] shown in Fig. 2(c). The architecture exhibits a more solid phase control than the MNMC because of the use of two feedforward transconductance stages. Moreover, the extra G_{mf} maximizes the amplifier bandwidth. A problem of the NMC structure is the presence of a right-half-plane (RHP) zero, which demands for a large output transconductance to ensure stability. The modified NMC scheme of Fig. 2(d) (NMCNR), which uses a nulling resistor, R_m , [5] sends the zero to infinite under certain conditions. The solution benefits the phase margin and improves bandwidth and slew-rate since smaller compensation capacitors can be used. A similar result is also achieved by another nonstandard NMC topology called *Damping Factor Control Frequency Compensation* (DFCFC) [6]. The topology, depicted in Fig. 2(e), removes the capacitive nesting structure and uses a damping factor control block to give rise stability when inner Miller capacitor is removed.

It can be observed that all the schemes of Fig. 2 suppose to have at the output of each amplifier the high impedance established by the inverse of the output conductance of MOS transistors. For a cascode implementation, on the contrary, there is a node with a much higher impedance and a second node with low impedance. That situation is more favorable because those two nodes affect the phase response at very different frequencies. Having cascode stages is possible even with low supply voltage, provided that they are not the output stage. The voltage allocated for the output swing can be conveniently used for biasing the cascode arrangement. In addition to an easier compensation there is a benefit on the gain, since the DC gain of a cascode is higher than the one of a simple inverter with active load.

For sampled-data schemes, in addition to gain and bandwidth, it is necessary to ensure a good slew-rate while consuming relatively low power. Unfortunately the compensation methods discussed above reduce the power effectiveness of the scheme because of the extra power consumed by transconductors and the power needed to drive the extra compensation capacitors. It is possible to boost the slew-rate with a dynamic control of the bias generators as done, for instance in [7]. Extra current flows through the compensation capacitor when needed. The method becomes complicated with nested capacitor schemes.

III. OP-AMP FOR NANOMETER TECHNOLOGIES

The study of the previous section indicates guidelines for the design of op-amps with nanometer technology. Namely, even if it is necessary using more than two stages, the requests for compensation and ensuring a good slew-rate response must be

Fig. 4. Complete schematic diagram of the proposed amplifier. (a) Two-stages amplifier. (b) Nested block with class AB stage.

Fig. 3. Proposed multistage amplifier topology.

carefully accounted for. The use of a cascode and an inverting amplifier gives rise to a gain that ideally is the product of the one of three inverting stages. However, the limited increase of the cascode output resistance caused by the low voltage available degrades the result. Therefore, it is necessary to compensate for that gain reduction possibly without using an extra gain stage.

The bias currents of the stages driving the compensation capacitors determine the slew rate. Class AB stages give rise to good slew rates because those currents dynamically change, but, unfortunately, the only effective class AB stage is the one described in [8]. Its implementation with low voltages is problematic because of the use of a mirrored or folded scheme. The extra non-dominant poles makes it more difficult compensating for the overall scheme. However, stages based on the same concept can benefit the slew-rate when they are used in a nested architecture.

Fig. 3 illustrates a possible implementation of the above concept. A class AB stage with two complementary outputs, in addition to the function performed in the nested schemes of Fig. 2, the complementary AB transconductance outputs boost the bias current thus increasing the current available for charging and discharging the compensation capacitance.

By inspection of the scheme the DC gain is

$$A_V = [(g_{m1} + g_{mf1})r_{o1} \cdot g_{m2} + g_{mf2}]r_{o2} \quad (1)$$

showing that the transconductance \$g_{mf1}\$ contributes to the gain. If \$g_{m1} = g_{mf1}\$ the gain increases by 6 dB without using

any extra gain stage.

The scheme of Fig. 3 can be the basis of other architectures with the cascade of more than three stages. They are possibly necessary when the obtained gain is lower than what required by the system specifications. The use of the techniques illustrated above enables compensation and the use of class AB transconductance stages in the feedforward paths sustains the slew-rate.

A. Transistor Implementation

In order to verify the effectiveness of the proposed design methodology, the scheme of Fig. 3 has been implemented and simulated at the transistor level using a 65 nm technology. The overall scheme, shown in Fig. 4, consists of three main blocks: input amplifier, second amplifier and nested block.

The input amplifier is a cascode. It can be telescopic or folded. Our scheme uses the telescopic version for reducing power and minimizing the parasitic capacitance of the non dominant nodes. Indeed the telescopic implementation is possible with a reduced \$V_{DS}\$ across the transistors \$M_{C5}\$ and \$M_{C6}\$. However, as will be describes shortly, the bias of the gates of \$M_{C3}\$ and \$M_{C4}\$ should dynamically change when the class AB stage boosts the current through \$M_{C5}\$ or \$M_{C6}\$. The second amplifier is a simple inverter with active load.

The nested amplifier uses as transconductance elements \$M_{C5}\$ and \$M_{C6}\$ of the first stage and \$M_3\$ and \$M_4\$ of the second stage. It just provides the driving voltages of those elements with p-channel and n-channel diode connected transistors. The input terminals of the class AB scheme are the ones of the first amplifier and their cross couples shifted versions. In this manner the control of the AB scheme doubles at the relatively power low cost determined by the two level shifts.

The class AB stage, in addition to the small signal benefits also boosts the current in the slewing conditions. The input pair of the first amplifier is completely unbalanced but one of the branches of the class AB drains a large current. In order to make effective the current boost for charging \$C_C\$ from the first stage side it is necessary, as mentioned above, to dynamically change the bias voltages \$V_{D1}\$ and \$V_{D2}\$. This is done by the bias network inside the class AB stage controlled by the boosted current. The compensation of the two stages main path is done with the conventional Miller capacitor with

Fig. 5. Simulated frequency response of the proposed amplifier with and without nested circuit.

Fig. 6. Simulated slew-rate performance of the amplifier with and without nested circuit. The input step amplitude is equal to 300 mV.

zero nulling resistor. However, since the second stage also uses the gate of M_3 and M_4 as auxiliary input terminals for the nested inputs it is necessary to add the extra compensation capacitors C_A for linking at high frequency the inputs of the second stage with equal sign.

IV. SIMULATION RESULTS

The multistage amplifier of Fig. 4 with suitable transistor sizing has been simulated with a 65 nm CMOS technology. All the transistors have the minimum length to emphasize the short channel limit. The supply voltage is 1.2 V. Fig. 5 compares the frequency response of the amplifier with and without the nested block. The use of the nested scheme improves the DC gain by approximately 9 dB. The result takes advantage of the doubling of the input signal at the class AB stage. The GBW increases by almost 3 times. The overall phase margin is 61 degrees, a suitable value for stable operation even with a unity gain configuration. Fig. 6 shows the transient response of the multistage amplifier for an input step of 300 mV of amplitude. The boosting technique heightens the slew performance from 22.5 to 84.5 V/μs, leading an improvement factor of about 3.5 times. The 0.1% settling time is also enhanced with 18 ns, almost two times faster respect to the one obtained without the boosting circuit. The output swing with a gain higher

Fig. 7. DC characteristic of the multistage amplifier.

TABLE I
SIMULATED OP-AMP PERFORMANCE

Parameter	Symbol [Unit]	Nested	–
Technology	CMOS	65 nm	
Power Supply	V_{DD} [V]	1.2	
Load Condition	C_L [fF]	250	
DC Gain	A_V [dB]	67.2	58.1
Slew-Rate	SR [V/μs]	84.5	22.5
Settling Time @ 0.1%	T_S [ns]	18	41
Unit Frequency	GBW [MHz]	321.5	115
Phase Margin	Φ_M [Degree]	61	88
Output Dynamic Range	DR [mV]	±450	±450
Power Consumption	P_W [μW]	240	217

than 60 dB is 0.15 V - 1.05 V, as shown in Fig. 7. Table I summarizes and compares the amplifier performance with and without the nested block.

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