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A Clock-Less 10-bit Pipeline-Like A/D Converter for Self-Triggered Sensors

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Abstract—In this paper, a novel 10-bit A/D converter based on a pipeline-like architecture specific for low-noise, self-triggered sensors, (e.g., X-rays and γ -rays spectrometry) is presented. The main innovative feature of the proposed A/D structure is the concept that, for a sampled input signal, a pipeline ADC may behave as a combinatorial logic and may operate without any timing signal (clock). The conversion is obtained asynchronously propagating the partial conversions and the residues through the various stages. This concept is validated by means of a prototype ADC fabricated in a standard 0.35 μm CMOS technology. The active area is 2.24mm², and it provides a conversion in 2.5 μs (i.e., it can operate with a 400 kS/s data rate) featuring an ENOB equal to 8.91.

Index Terms—Analog–digital conversion, asynchronous logic circuits, gamma-ray spectroscopy, spectroscopy, X-ray applications.

I. INTRODUCTION

X-RAY and γ -ray spectrometry is gaining relevance in many fields, ranging from astronomy to medicine. In such spectrometers, a large array of semiconductor sensors is used to detect events, which occur randomly with Poissonian distribution. In order to build an energy spectrum, the energy of each event has to be measured with a resolution of the order of 8–10 b. Thus, the sensors are typically connected to very-low-noise front-end circuits, which provide an output dc voltage proportional to the energy of the event (through a peak-and-hold circuit) as well as a trigger signal that informs the system that an event has occurred. Therefore, spectrometers are a typical case of self-triggered application. The integrated circuits for X-ray or γ -ray spectrometers available so far [1], [2] provide as output a static analog signal proportional to the energy of the event, while A/D conversion of this static analog signal is performed externally, typically with multichannel analyzers. The use of an external ADC introduces some noise sources due to the coupling to the analog interfacing. However, the clock signal needed for on-chip A/D conversion would introduce significant on-chip noise through the substrate that

would dramatically affect the accuracy performance of the front-end circuit. On the other hand, A/D converters, which do not require a clock signal if the input signal is already sampled, such as full flash A/D converters, do not achieve a sufficient accuracy for spectrometry. Therefore, a fast and accurate A/D converter capable of operating without a clock signal would be extremely useful to achieve high-performance fully integrated X-ray or γ -ray spectrometers. These devices would be beneficial especially for astronomical applications on satellites, where size and weight have to be minimized.

The innovative clock-less A/D converter presented in this paper allows one to solve the above bottleneck in the design of self-triggered sensor applications. The proposed A/D architecture is based on the pipeline structure, which can achieve a good accuracy (up to 10 bits). The typical pipeline architecture has been properly modified in order to operate without the clock signal. The proposed structure requires that the input signal has to be sampled and a trigger signal is provided to start the conversion. These requirements are fully satisfied by the self-triggered sensor applications, among which Fig. 1 reports a possible block diagram.

The main innovative feature of the proposed structure is that this pipeline ADC behaves as combinatorial logic. In the data converters so far, the task of a clock signal is to give proper timing to the sequence of operations required to achieve the conversion from the analog to the digital domain or *vice versa*. If it is assumed that each operation is completed within a certain time slot, then the clock can be removed, thus obtaining the proposed structure. The proposed novel concept requires an improved block design in order to guarantee timing operation as it will be discussed in the following.

This paper is organized as follows. After this introduction, Section II presents the clock-less concept and the relative modification of the ADC building blocks. Section III gives details about the circuit design of the ADC. Section IV describes the realization of a silicon prototype that demonstrates the validity of the proposal. Layout issues and experimental results are reported. Section V concludes the paper.

II. CLOCK-LESS PIPELINE-LIKE ARCHITECTURE

The architecture of the proposed clock-less pipeline-like A/D converter is shown in Fig. 2. This structure appears as a standard pipeline ADC. The architecture consists of nine conversion stages, an array of flip-flops, and a ripple-carry adder, which provides the digital correction to reduce threshold voltage variation sensitivity. Each of the first eight stages provides 1.5 bits of partial conversion, while the last one is a 2-bit flash ADC. The output bits of the nine stages are sampled by a register of flip-

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Fig. 1. Typical application of the proposed A/D converter.

Fig. 2. Block diagram of the A/D converter.

flops controlled by the end-of-conversion (EoC) signal, which is a delayed version of the start-of-conversion (SoC) signal, and added with a ripple-carry adder (RCA) in order to achieve the final ten output bits with digital error correction [3]. The schematic diagram of one of the first eight stages as well as that of the last stage are shown in the insets of Fig. 2. Each 1.5 bit conversion stage consists of a flash ADC with a resolution of 1.5 bits, a DAC, an adder, and a gain stage with a gain equal to 2.

The key requirement of the circuit design is to ensure that the overall ADC data conversion ends within the scheduled time slot. The most critical point to achieve this target is the calculation of the residual error at each 1.5 bit stage for the following stage, which is operated using the results of the previous stage (with the eventual error propagation). The overall data conver-

sion time slot is obtained adding the residual calculation time of each of the nine stages of conversion.

The main difference with respect to a standard pipeline ADC is within the comparator and ADC functionality and, as a consequence, in the circuit design.

The general functionality of a comparator in a pipeline ADC is two-fold:

- 1) to take a decision within the available time slot;
- 2) to maintain the output signal for the needed time for the following stage operation.

These two features in a *standard* clocked comparator are realized by means of the following solutions.

- 1) The comparator uses a structure composed by a preamplifier and a latch. The latch operates on an amplified signal

Fig. 3. Output code applying a constant input with a 1-LSB amplitude noise added (a) without and (b) with hysteresis.

(the preamplifier output) and embeds a positive feedback to increase the gain and speed-up the decision.

- 2) The clock signal commutes between different states of a register that reads the latch output signal during one clock phase and properly maintain this signal during the other clock phase.

The operations of these two blocks are strictly correlated with the use of the clock signal that drives them. In the proposed structure, the clock is not available. As a consequence, the two above features have to be realized with an alternative approach. In this paper, a possible solution is proposed for the two points, as follows.

- 1) The comparator structure uses only an open-loop amplifier stage, whose output will be used as a digital signal. Such an amplifier has to feature very large gain (much larger than the preamplifier of a clocked comparator) to guarantee a decision even for the minimum signal within the available time slot and to prevent having metastability of the comparator.
- 2) Since the comparator input signal could, in principle, change during operation (due to noise or disturbances), due to the comparator open-loop operation, the comparator output signal could change with a consequent error in the following stage operation. A proper hysteresis has then been implemented in the comparator. Thus, once a decision is taken, the comparator does not change its output signal. The exact value of the hysteresis will be analyzed later on.

These two arrangements guarantee the functionality of the overall pipeline-like clock-less ADC. The validity of the proposal is demonstrated in Fig. 3 that shows the output code while applying a constant input with a 1-LSB amplitude noise added, with and without hysteresis (simulations in Simulink). No effect of the applied noise is observed in the ADC using the hysteresis. On the other hand, without hysteresis, the output code shows a ripple much larger than 1 LSB, reducing ADC performance.

As a result of the above considerations and proposals, the 1.5-bit ADC within each pipeline stage is realized with two open-loop comparators with hysteresis [4], which compare the input signal with two thresholds.

Fig. 4. Four different types of hysteresis simulated.

Notice that the digital correction allows the A/D converter to operate properly even in the presence of a large threshold error. This is greatly exploited in this solution, since hysteresis can be considered as a threshold error. The form and the value of the hysteresis have been chosen after widely simulating in Simulink an ideal model of the A/D converter with different possible solutions of hysteresis in the two 1.5-bit ADC comparators. In this analysis, the actual full-scale signal of the ADC ($2 \cdot V_{\text{REF}} = 1.2V_{\text{DD}}$) is used. In this case, the nominal values of the threshold voltages of the two comparators are placed at $V_{\text{REF}}/4 = +150 \text{ mV}$ and $-V_{\text{REF}}/4 = -150 \text{ mV}$, respectively.

Four different forms of hysteresis have been simulated, the schemes of which are shown Fig. 4, and are:

- aligned to the bottom on both the comparators of the 1.5-bit ADC (case 1);
- aligned to the top on both the comparators of the 1.5-bit ADC (case 2);

Fig. 5. Comparator response in the process corners.

TABLE I
MAXIMUM VALUE OF THE HYSTERESIS

	Simulation results			
	Case1	Case2	Case3	Case4
Maximum value of hysteresis	150mV	140mV	150mV	140mV

- aligned centred on both the comparators of the 1.5-bit ADC (case 3);
- aligned to the bottom on the V_{ThH} -comparator and aligned to the top on the V_{ThL} -comparator (case 4).

Table I shows the maximum value of the hysteresis allowed in the four cases to ensure either DNL or INL to be within -0.5 LSB and 0.5 LSB.

As a consequence, the form of the hysteresis has been selected considering other implementation issues. In this design, a centered hysteresis (case 3) around the threshold voltage level has been used because of its layout symmetry that gives the design robustness.

On the other hand, the amount of the hysteresis has been selected with functionality considerations. In the above analysis, for all of the cases, the structure performance becomes critical for a hysteresis larger than 150 mV. These values corresponds to the considerations that the hysteresis has to be lower than the reference voltage of the comparators, otherwise the digital correction is no longer effective. In fact, since the digital correction technique corrects threshold errors up to $V_{REF}/4$ ($= 150$ mV for $V_{REF} = 0.6$ V) [3], all of the above cases respect the 1.5-bit per stage theory of an A/D pipeline converter. In this design, the amplitude of the hysteresis is set to 100 mV as a tradeoff between large robustness for the clock-less operation (achieved with a large hysteresis) and good digital correction effectiveness (achieved with small hysteresis).

Simulations in the worst case were made for the comparator to be sure that the value of the hysteresis does not exceed the maximum tolerable value of $V_{REF}/4$ ($V_{REF} = 0.6$ V). Fig. 5 shows the falling decision voltage of the V_{ThL} -comparator, ideally equal to 1.3 V, in several process corners. It can be noticed

that the comparator decision is almost the same in every process corner. The variation of the decision voltage is around 25 mV, which stays in the limits of the digital correction. Thus, the nominal value of 100 mV guarantees that, for any worst case (e.g., aging, temperature, or technology), the hysteresis is lower than that of $V_{REF}/4$.

The only digital signal in the proposed clock-less pipeline-like ADC is the SoC that is generated by the experiment trigger. A second control signal is the EoC, which is obtained by delaying the SoC signal through an analog block, consists of an RC network followed by a comparator equal to those used in the main ADC. The value of delay is equal to T_{sample} and has been chosen in order to match the delay of the pipeline chain. This signal is used to strobe the digital output of each stage and to control the digital correction section.

III. CLOCK-LESS PIPELINE-LIKE CIRCUIT DESIGN

Here, a detailed description of the most important circuit solutions is given.

The schematic diagram of the comparator is shown in Fig. 6. The key point regards the hysteresis amount, as previously analyzed, that has been implemented at the transistor level. The proposed comparator operates as follows where the value of the hysteresis is proportional to the ratios β_{10}/β_3 and β_{11}/β_4 .

Assume that initially the input voltage V_{In} is much lower than the threshold voltage of the comparator. In this case, all of the current flows through MN1 and MP3; MP11 and MP4 are off, and consequently the output voltage is low. MP10 is on also, but no current is flowing in it. Initially, when the input voltage increases, nothing happens until $V_{In} \cong V_{Th}$. At this point, some current starts to flow into MN2 from MP10 and I_{NM1} starts to decrease, so the following relations can be written:

$$I_{MN2} = I_{MP10} = \alpha_r I_{MP3} \quad (1)$$

$$I_{MN1} + I_{MN2} = I_{MN5} = I_{Bias} \quad (2)$$

$$I_{MN1} + \alpha_r I_{MP3} = I_{Bias} \quad (3)$$

$$I_{MN2} = \alpha_r I_{MP3} \propto (V_{In} - V_{Th})^2 \quad (4)$$

Fig. 6. Schematic circuit of the comparator.

Fig. 7. The adder and gain stage. (a) Noninverting. (b) Inverting.

where α_r is the ratio β_{10}/β_3 , and subscript r stands for *raising*. If the input voltage is increased further on, MN2 demands for more current that can come only from MP10 that mirrors I_{MP3} with the ratio α_r , while I_{MP3} is decreasing. At a certain point, MP10 ($\alpha_r I_{MP3}$) cannot validate (2), because $I_{MP3} = I_{MN1}$ is too low, and consequently MP4 goes on, providing the current MN2 is asking for [see (4)]. Therefore, the output voltage of the comparator becomes high as follows:

$$I_{MN1} + I_{MP4} = I_{Bias}. \quad (4)$$

The last value of V_{In} that verifies (2) is the raising-decision threshold, and the difference $V_{In} - V_{Th}$ is the value of the raising-hysteresis that is proportional to α_r . Thus, its value can be changed by the α_r parameter: the higher α_r is, the longer (2) is verified and higher the raising-hysteresis that validates (3) is. It is important to point out that (1)–(3) are true only when $V_{In} \cong V_{Th}$ and (4) is true only when the output voltage is high.

The same operations happen symmetrically in the falling decision: the falling hysteresis is determined by α_f that is the ratio β_{11}/β_4 , and subscript f stands for *falling*. MP11, MP4, and MN2 are on while MP3, MP10, and MN1 are off.

The transistor sizes of the comparator are shown in Table II. The gain of this stage is about 30 dB. This is not sufficient to

TABLE II
DIMENSIONS OF THE COMPARATOR'S MOSFET

Transistors	W/L ($\mu\text{m}/\mu\text{m}$)
MN1, MN2, MP3, MP4	35/0.35
MN4, MN7, MNBias, MP6, MP8	40/0.35
MN5	50/0.35
MP10, MP11	100/0.35

guarantee a decision within the available time slot for the minimum input signal. Two digital inverters have then been added at the comparator output to guarantee the required gain.

The MDAC subtracts the voltage generated by the DAC from the input signal, generating the residual voltage, which is amplified by two, and represents the input signal of the next stage. Also, in this stage, the use of a nonclocked structure results in novel implementation solutions. The adder and the gain stage can be realized with an operational amplifier in closed-loop configuration with two possible solutions, as shown in Fig. 7. The designed solution is the noninverting one, as will be discussed in Section IV. The two resistors used in the feedback path are of the same value and equal to 100 k Ω . This value is sufficiently large to avoid a significant increase of the operational amplifier power consumption and small enough to require reasonable area

Fig. 11. Microphotograph of the chip.

in Fig. 7(b)], since it achieves a higher speed. This higher speed (due to a larger feedback factor) is obtained at the cost of the higher operational amplifier input signal swing. The feedback factor is $1/2$, and this gives a closed-loop bandwidth (12.5 MHz) equal to $1/2$ of the operational amplifier unity gain bandwidth (about 25 MHz). The 9.5 MHz pole for a 9 bit settling accuracy leads to a response time of $0.1 \mu\text{s}$. The cascade of nine such stages then leads to a $0.9 \mu\text{s}$ delay, which is consistent with the overall conversion time verified in the experimental results.

It is useful to point out that the proposed structure could have a potential issue of error propagation due to the fact that the comparator could decide far before the input signal is fully settled (e.g., because of the ripple of the signal during its settling). This could happen because, as mentioned in Section II, the comparator structure is continuous-time and hence it can switch at any time. From circuit simulations in Cadence environment that take into consideration this aspect (i.e., the ripple of the signal during its settling), this error does not affect the performance of the A/D converter, thus leading in simulation to an ENOB of 9.7 bits.

The conversion process with N cascaded stages results in a limit of the sampling frequency that is N times lower than a clocked pipeline A/D converter with the same settling time per stage.

On the other hand the proposed A/D converter, although it features a competitive power consumption in its application field (i.e., event-triggered application), burns most of the power just to maintain the residue until the conversion process is finished, while a clocked pipeline A/D converter, with the same frequency and resolution, neglecting the latency (which is anyway important in event-triggered applications), would consume, in first approximation, N time less than the clockless solution.

IV. EXPERIMENTAL RESULTS

The proposed clock-less pipeline-like ADC concept has been demonstrated by the realization of a prototype in a standard $0.35 \mu\text{m}$ CMOS technology. Fig. 11 shows the microphotograph of the active area whose size is 2.24 mm^2 . The eight 1.5-bit stages, the last 2 bit flash ADC, the feedback resistor arrays, the operational amplifier bias circuit, the comparator bias circuit, the digital part, and the resistor arrays for the reference voltages can be observed. A particular issue of this realization is that the input signal of the target application, X-ray and γ -ray spectrometry, is single-ended. For this reason, the full ADC topology uses single-ended structures, and this gives additional worth to the achieved ENOB $\cong 9$ bit.

A. Layout Issues

In the layout design, the flash ADC is much smaller than the 1.5-bit stages because it does not include the operational amplifier and the feedback resistors. Particular attention was devoted to the design of the resistors used in the closed-loop amplifier because they determine the accuracy of the generated residue, and then any inaccuracy is reflected in the overall ADC performance. To achieve this target, each resistor consists of eight $12.5 \text{ k}\Omega$ stripes for a total value of $100 \text{ k}\Omega$ with dummy resistors around to minimize the border effects [5]. High-resistive polysilicon was used to realize the resistors because it features the lowest mismatch factor among the materials available in the used CMOS technology. The mismatch between two equal resistors can be written as

$$\sigma\left(\frac{\Delta R}{R}\right) = \frac{A_R}{\sqrt{WL}} \quad (5)$$

where W is the width of the resistor, L is the length, and A_R is the mismatch parameter (for the high-resistive polysilicon used, $A_R = 7 \mu\text{m}$). To calculate the maximum allowed mismatch between the two resistors of the first stage of the pipeline structure, which is obviously the most critical since it has to guarantee 9 bit, the following relation was used for a full scale ($= 2V_{\text{REF}}$) of 1.2 V :

$$\text{Mismatch}_{\text{max}} = \frac{1.2}{2^9} = 0.00243. \quad (6)$$

As a consequence, a maximum mismatch of 2.4% can be tolerated. The width and the length of the resistors are then determined by using the following relation:

$$\sigma\left(\frac{\Delta R}{R}\right) = \sigma\left(\frac{8\Delta r}{8r}\right) = \sigma\left(\frac{\Delta r}{r}\right) \quad (7)$$

where r represents one of the eight $12.5 \text{ k}\Omega$ stripes of each resistor. Choosing $13 \mu\text{m}$ as width and $130 \mu\text{m}$ as length (leading exactly to $12.5 \text{ k}\Omega$), the obtained value of σ is

$$\sigma\left(\frac{\Delta R}{R}\right) = \frac{7}{\sqrt{13 \cdot 130}} = 0.17. \quad (8)$$

Therefore, the mismatch on the ratio between the two resistors R in Fig. 7, which determines the gain G of the residue amplifier, is given by

$$\begin{aligned} \sigma\left(\frac{\Delta G}{G}\right) &= \sqrt{\sigma\left(\frac{\Delta R}{R}\right) + \sigma\left(\frac{\Delta R}{R}\right)} \\ &= \sqrt{2}\sigma\left(\frac{\Delta R}{R}\right) = \sqrt{2} \cdot 0.17 = 0.24 \end{aligned} \quad (8)$$

Fig. 12. DNL.

Fig. 13. INL.

which is lower than the maximum allowable value.

B. Measured Performance

The proposed A/D converter provides a conversion within a $2.5 \mu\text{s}$ time-slot after the SoC signal. This allows a possible data rate of 400 kS/s.

To measure either static (INL and DNL) or dynamic (SNR and ENOB) performance parameters of the A/D converter, an external sample and hold was used to match the configuration of the final spectrometry application. Figs. 12 and 13 show the static performance of the converter: the DNL is within -1.2 and 1.2 LSB while the INL is within -2.5 and 2.5 LSB. This satisfies the application requirement of 8 bits.

Fig. 14 shows the dynamic performance. A typical FFT spectrum measured with an 80 kHz input sine wave at 400 kS/s is

Fig. 14. Output spectrum for a 80 kHz full-scale input signal.

reported. Notice that operating with a ratio $f_{\text{in}}/F_s = 1/5$ corresponds to having large steps between consecutive samples, and this could be critical for a clock-less ADC. In addition, an external sample-and-hold is not perfectly suitable for this timing-less converter. However, in this case, an $\text{SNR} = 55.4$ dB (i.e., an $\text{ENOB} = 8.91$ bit) is achieved, demonstrating the validity of the proposed ADC concept and implementation.

The power consumption is 14 mW from a 2.3 V power supply. Nonetheless, this power amount is significantly large with respect to other 10 bit 400 kS/s ADC, and this value is competitive for the considered application in comparison with alternative solutions that should have larger power consumption for exhibiting the same performance of environment clarity achieved here with the clock-less concept.

V. CONCLUSION

In this paper, a novel A/D converter concept for low-noise, self-triggered applications is proposed. The main innovative feature of this A/D converter is that, assuming that a sampled input signal is provided, it operates without the clock signal, which is usually a source of severe disturbances in low-noise circuits. The A/D converter in a standard $0.35 \mu\text{m}$ CMOS technology with an active area of 2.24 mm^2 provides a conversion every $2.5 \mu\text{s}$ (400 kS/s) and consumes 14 mW from a 2.3 V power supply.

REFERENCES

- [1] S. Baba, K. Ohmori, Y. Mito, T. Tanoue, S. Yano, K. Tokumori, F. Toyofuku, and S. Kanda, "Recent development of radiation measurement instrument for industrial and medical applications," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 458, no. 1, pp. 262–268, 2001.
- [2] M. Prydderch and P. Seller, "A 16 channel analogue sparse readout IC for integral," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf.*, 1994, vol. 1, pp. 65–68.
- [3] R. van de Plassche, *Integrated Analog to Digital and Digital to Analog Converters*, 2nd ed. Boston, MA: Kluwer, 2003.
- [4] F. Maloberti, *Analog Design for CMOS VLSI System*. Boston, MA: Kluwer, 2001.
- [5] A. Hasting, *The Art of Analog Layout*. Upper Saddle River, NJ: Prentice-Hall, 2005.

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