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A Micropower Chopper—CDS Operational Amplifier

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Abstract—A low-power spur-free precision amplifier, which uses input chopping and correlated double sampling for demodulation, is presented. This circuit employs an AC coupling between the first and the second stage that removes the first stage offset without causing ripple. The input rail-to-rail circuit, fabricated in a mixed 0.18–0.5 μm CMOS technology, operates with supply ranging from 1.8 V to 5 V. The circuit achieves a simulated 168-dB DC gain with an overall current consumption of 14.4 μA . The measured offset voltage over the available samples results in a distribution with 2- μV standard deviation. The obtained input noise density at low-frequency equal to 37 nV/ $\sqrt{\text{Hz}}$ gives a 5.5 noise efficiency factor.

Index Terms—Chopper technique, CMOS analog integrated circuits, offset cancellation, operational amplifiers, ripple reduction.

I. INTRODUCTION

THE tiny signals processed by many instrumentation applications require large amplification. Accordingly, the operational amplifier needs very high gain (in the 100–140 dB range), extremely low offset, and very low input noise. Often the signal bandwidth is low, thus leading to limited speed requirements. Typically, the needed unity gain frequency is low. In addition, the power consumption for portable applications must be in the range of few tens of μW .

Both auto-zero architectures, [1], and chopper stabilized schemes, [2]–[5], meet the low offset requirement. However, since a conventional chopper-stabilized amplifier is not able to adequately remove the ripple caused by signal demodulation, the auto-zero method, depending on system requirements, can be preferred. Nevertheless, the auto-zero is not suitable for low power because it requires storing offset on a capacitor, whose value, because of the kT/C requirement, can be relatively large. In turns, large storing elements typically increase power because driving large capacitive loads augments the bias current.

Using on chip lowpass or notch filters attenuates spurs at multiples of the chopping frequency caused by signal demodulation. Examples of sampled data and continuous time on-chip notch filters are given in [6]–[8].

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The method of this precision amplifier avoids any ripple spurs generation by combining the chopper technique and the correlated double sampling (CDS) method, [9]. CDS replaces, as reported in [4], the signal demodulation while the AC coupling removes the offset of the first stage, amplified by its DC gain. It does not saturate the output thanks to a careful layout and a novel preamp scheme, which incorporates a bandpass filter, as done in [2], [10], and [11]. Given that the amplifier is intended to be used only in applications with closed loop gain higher than 10, it is decompensated to optimize power dissipation. A CDS scheme introduces a delay, typical of any switched capacitor solutions, [6]. However, the limit is not critical for low band input signals.

This design uses high chopping frequency to tradeoff the folding of noise over the Nyquist range and the input current. The obtained 1 nA over the temperature range is however acceptable for expected applications.

This paper is organized as follows. Section II briefly reviews and discusses conventional solutions for offset and $1/f$ noise cancellation. Sections III and IV describe the proposed method and illustrate the first gain stage. Section V discusses implementation details and gives a noise analysis. Section VI presents the measurement results. Finally, Section VII gives some conclusions.

II. AUTO-ZERO AND CHOPPER METHOD FEATURES

The cancellation of offset and low-frequency noise is conventionally obtained with auto-zero, [1], or chopper methods, [2]–[6]. With the simple cascade of multiple stages A_1 , A_2 , and A_3 , the input referred offset is $V_{os1} + V_{os2}/A_1 + V_{os3}/(A_1A_2)$. The contributions of following stages become the residual offset when V_{os1} is cancelled. The advantages and drawbacks of auto-zero and chopper techniques are briefly described here to have a term of comparison with the method used in this design.

Auto-zero uses two phases: one for sampling and store on a capacitor offset and noise, the other for normal operation. During the amplification phase, the input subtracts the stored error to obtain offset-free operation. The method is substantially sampled-data; moreover, input is not processed during the sampling phase. The use of a ping-pong arrangement, [12], [13], avoids that limit. However, the circuit complexity and the power dissipation increase.

The auto-zero method highpasses the low-frequency noise (dominated by the $1/f$ term) by a $(1 - z^{-1})$ sampled data transfer function. Sampling, however, at least doubles the power of white noise, [13], being its samples uncorrelated. Therefore, in order to keep unchanged the noise spectrum, the transconductance of the first gain stage that mainly determines the white noise must increase. With input pairs in sub-threshold or saturation region, doubling g_m requires to increase the bias current by 2 or 4, respectively.

Fig. 1. Chopper technique basic scheme.

The presence of sampled capacitance C limits the total noise power in the Nyquist interval to kT/C . This noise power is referred to the input divided by an equivalent gain. For schemes with auto-zero at the input, the equivalent gain is 1 or very low to ensure effectiveness. Thus, the capacitance value must be high and power consumed by its driving stage relatively high.

The chopper technique transposes the input signal to high frequency by modulation, as done by the multiplier M_1 of Fig. 1(a), and then demodulates it back to the baseband with the multiplier M_2 after amplification. The modulating signal is a square-wave signal, $m(t)$, with period $T = 1/f_{\text{chop}}$. After the first modulation, offset and $1/f$ noise (V_{os} and V_n , respectively) corrupt the signal, but they are transposed to high frequency by the action of M_2 . Fig. 1(b)–(d) depicts the spectra of the signal involved in the relevant points of the processing chain. The $1/f$ frequency noise added to input of A_1 , modulated by M_2 and replicated at multiple of f_{chop} , is possibly lowpass filtered by the finite bandwidth of A_1 , but the residual terms are normally not acceptable. Many architectures use additional lowpass filters to reduce the amplitude of those spurs. The incomplete cancellation remains a problem for some precise applications. However, an advantage of chopping compared to auto-zero is that it does not suffer from noise aliasing.

Solutions proposed in [5], [7], and [8] address the ripple problem. Another effective low-power solution uses a sampled data notch filter after the second modulator M_2 , [6]. Since the frequency of the switched capacitor filter is f_{chop} , there is an automatic tuning of notch position and spur frequencies. Another method uses a jittered chopper control, [14]. The jitter blurs the spurs and spreads their power around the chopping frequency and its multiples. The method increases the noise floor and, therefore, establishes a tradeoff between noise floor level and residual spurs. Ripple tones are not generated at all if the offset of A_1 is cancelled. This is done in [15] by a local zeroing feedback before M_2 . Other solutions, [16]–[18], combine the above techniques and use auto-zeroing and chopping.

III. CHOPPER-CDS ARCHITECTURE

This design uses a chopper at input, but avoids spur tones at f_{chop} and its multiples by replacing M_2 with a correlated double sampler (CDS). The method is well known being used

Fig. 2. Simplified single-path chopper-CDS block diagram.

to cancel offset [1], [4]. Fig. 2 shows a simplified block diagram of the architecture together with the driving phases. The second gain stage, A_2 , increases the overall gain. The scheme foresees chopping of input signal before the offset and $1/f$ noise (V_{os} and V_n , respectively) addition. Assuming that offset and $1/f$ noise do not saturate the amplifier, the AC coupling almost removes their contribution. The correlated double sampling block (CDS) detects the signal. The inset of Fig. 2 schematically describes the CDS operation. The switch controlled by the phase Φ_1 precharges the capacitor C_{cds} to the voltage at output of A_1 . During the complementary phase, capacitor C_{cds} is in series with C_s , supposed initially discharged. Notice that sampling of C_{cds} occurs just before chopping, when the switching transient is extinguished. Thanks to the chopping of the input, the output voltage of A_1 , V_o , during Φ_1 and Φ_2 , is

$$V_o(\Phi_1) = A_1(-V_{in}(\Phi_1) + V_{os} + V_n(\Phi_1)) \quad (1)$$

$$V_o(\Phi_2) = A_1(V_{in}(\Phi_2) + V_{os} + V_n(\Phi_2)). \quad (2)$$

Therefore, during Φ_2 , the voltage across C_s becomes

$$V_{cs}(\Phi_2) = C_{\text{cds}} \frac{-V_o(\Phi_1) + V_o(\Phi_2)}{C_{\text{cds}} + C_s} \quad (3)$$

that, using (1) and (2), yields

$$V_{cs}(\Phi_2) = \frac{A_1 C_{\text{cds}} [V_{in}(\Phi_1) + V_{in}(\Phi_2) - V_n(\Phi_1) + V_n(\Phi_2)]}{C_{\text{cds}} + C_s} \quad (4)$$

showing a sampled data processing function $(1 + z^{-1})$ for the input signal, while the $1/f$ noise passes through the highpass function $(1 - z^{-1})$. Moreover, since the method does not involve any chopping, no coupled ripple results.

Since the control of A_2 occurs during both phases with a fully differential signal, this design uses four CDS structures, as shown in Fig. 3, working in ping-pong fashion, and employs both amplifier outputs. The output voltages charge two of the CDS capacitors during one phase and the other two during the other phase. While two CDS capacitors are charged, the others discharge the stored signal into the virtual ground. The switching of capacitors in the CDS section gives rise to spur charge injection. Since the scheme is fully differential, the limit mainly causes a common-mode signal. Mismatch between switches generates a differential term that is referred to the input divided by A_1 . Notice that capacitor C_{cds} and stored capacitor C_s share the charge injected by switches $S_5 - S_{12}$. Their effect is less critical than the one due to switches $S_{13} - S_{16}$ connected to virtual ground of the following stage.

Fig. 3. Chopper and CDS fully differential schematic diagram.

Fig. 4. Main offset contributions in a folded cascode scheme.

IV. PREAMPLIFIER A_1

The scheme of Fig. 3 uses an AC coupling between the output of A_1 and the CDS circuitry. This naturally removes offset, but opens the overall loop at DC. Therefore, the offset of A_1 shows up at the output amplified by the DC gain of the stage. This is not a problem if the obtained voltage is in the A_1 linear region of operation. The large gain of A_2 makes the dynamic swing of output A_1 very small; therefore, it is just required to keep the output of A_1 , $V_{os1}A_1(0)$, below its saturation level. The offset of a conventional gain stage, like the folded cascode of Fig. 4, depends on the contributions V_{os1} , V_{os2} , and V_{os3} caused by mismatches of the related transistor pairs and bias controls. The output offset is

$$\begin{aligned} \Delta V_{OUT} &= G_1 V_{os1} + G_2 V_{os2} + G_3 V_{os3} \\ &= g_{m1} \left(V_{os1} + \frac{g_{m3}}{g_{m1}} V_{os2} + \frac{g_{m11}}{g_{m1}} V_{os3} \right) R_{OUT} \quad (5) \end{aligned}$$

where R_{OUT} is the output resistance. The input referred offset is typically dominated by the input pair. Therefore, supposing $g_{m1} \gg g_{m3}$ and g_{m11} , G_1 becomes higher than G_2 and G_3 , making small the effect of V_{os2} and V_{os3} . The same holds for

Fig. 5. Simplified diagram of the used first stage structure.

Fig. 6. Input signal gain of the amplifier.

the noise contributions. The strategy used by this design is to reduce all the three terms of (5). The schematic diagram of Fig. 5 illustrates the methods. Since what matters is the gain at f_{chop} and not the one at DC, the scheme realizes a highpass response with low gain at DC and high gain at the chopping frequency. This feature permits high signal preamplification without risk of saturation. The capacitor C between the sources of M_1 and M_2 is low impedance at the chopping frequency, thus establishing a common source condition. Therefore, at the chopping frequency, the gain G_1 is $g_{m1}R_{OUT}$, as shown in Fig. 6. At DC, the capacitor C disconnects the sources making a source follower each input branch. Thus, the low-frequency gain becomes R_{OUT}/R_E , where R_E is the output resistance of the bias generators. The response has a zero and a pole (at $g_{m1}/2\pi C$). Since the chopping frequency must be higher than the pole, C must be more than $g_{m1}/(2\pi f_{chop})$. Large transient differential signals just give rise to slewing of the preamplifier. Large changes of the common mode can bring in triode the current generators

Fig. 7. Block diagram of the proposed amplifier.

Fig. 8. Detailed schematic diagram of the used first stage with bandpass response.

of the input pair. The use of complementary input stages, as discussed shortly, addresses the limit.

The reduction of the DC value of G_1 makes it comparable with gains G_2 and G_3 (which are equal to about 10). They are relatively low. However, in worst case situations, the amplified offset at the output of A_1 can still be too large. To further reduce their effect, we use local feedback loops between the outputs and the auxiliary inputs, M_{11} and M_{12} . The passive feedback is lowpass and band-reject. Therefore, the feedbacks operate at low and high frequencies, but they are ineffective in the switching region. Namely, at DC, the feedback significantly reduces R_{OUT} and, hence, the gains G_1 , G_2 and G_3 . Moreover, it operates as common mode feedback. A possible mismatch in the frequency response is not critical provided that the low-frequency gain is close to 1.

V. CIRCUIT DESIGN

A mixed 0.18–0.5- μm CMOS process, with 5-V option, dual poly 6-metal layers and zero threshold transistors, has been used for the design of the complete block diagram shown in Fig. 7. A folded cascode second stage drives the class AB output stage. A suitable control of the bias section limits the quiescent current

of the AB stage below $2\text{ }\mu\text{A}$. The class AB output uses the same scheme proposed in [19]. Moreover, since simulation results show that reference currents increasing with temperature compensate for the temperature dependence of the residual offset, all the references are the mirroring of an untrimmed PTAT (proportional to the absolute temperature) current source [20].

The value of the chopping frequency, 500 kHz, depends on various tradeoff considerations. Having high chopping frequency reduces the value of the capacitor coupling the input sources. Moreover, high chopping rate spreads the kT/C noise generated in the CDS network over a large frequency range. However, high chopping frequency increases the power consumption and reduces the input impedance. This, in turns, increases the input current. The chosen frequency enables the given benefits, while keeping low the power consumption. The input current associated with the charging and discharging of the amplifier input capacitance by the input chopping is at an acceptable level (less than 1 nA over the temperature range). An on-chip 1-MHz ring oscillator determines all the needed clock phases.

Fig. 8 details the circuit schematic of A_1 . It uses complementary input stages to ensure a rail-to-rail input. Moreover, zero

Fig. 9. Simulated response of the first stage amplifier (supply voltage = 1.8 V) and noise folding.

threshold transistors (M_{11} , M_{12} , M_{19} , and M_{20}) optimize the dynamic range of input and output branches. The coupling capacitors C_N and C_P , required to ensure low impedance at the chopping frequency, have a large value, 30 pF, but the corresponding silicon area is still affordable. Notice that despite the high value of capacitances, there is no increase in power consumption. The inner loops use unity gain buffers (source followers) to drive a passive lowpass filter cascaded with a twin-T band reject filter. The lowpass filter, set at about 2 kHz, is a simple RC with $R = 15 \text{ M}\Omega$ and $C = 6 \text{ pF}$. The AC coupling of first and second stage does not constrain the output common mode of A_1 set to 0.9 V. It is the DC shift of the unity gain buffers and the V_{GS} of transistors M_{23} – M_{24} . This almost fixed value enables us to realize the 15-M Ω resistor with a transistor. The twin-T network needs lower resistor values and uses high-resistive poly. The overall area of the band-reject filter is $200 \mu\text{m} \times 200 \mu\text{m}$. Fig. 9 shows the simulated Bode diagram of A_1 in the worst case (supply voltage = 1.8 V). The DC gain is -23 dB ; the gain at 500 kHz is about 50 dB. The peak of the gain (about 53 dB) is at 340 kHz. The use of a chopping frequency higher than the peak optimizes the noise, as discussed below. The transconductance of the input transistor with 1.2 μA is 31.2 μS . At 1.8-V supply voltage and input common mode at 0.9 V, R_E is at its minimum value, about 1 M Ω .

The clock feedthrough of all switches, driven by nonoverlapping phases, and their mismatch must be carefully controlled. Among them, the switches S_{13} – S_{16} of Fig. 3 directly connected to virtual ground of the following gain stage. Thus, the switches layouts must be properly interdigitated and have common centroids. The common mode of the second stage input is 1.5 V. This enables the use of 0.18- μm n-channel switches, driven at 1.8 V, to reduce charge injection. A clock tree with a limit in the current that inverters can provide obtains controlled rising and falling edges, thus reducing glitches.

The pole splitting network of Fig. 7 with zero nulling resistor obtains a good control of the phase margin that should be better than 60 degrees for gains higher than 20 dB. Having a decompensated scheme is not a real limit because this operational amplifier is supposed for high gain. A lower compensation capacitance allows the designer to spare power that is possibly invested in the input stage to reduce the input noise.

The overall scheme has been extensively simulated with the periodic steady-state and periodic noise analyses options of

Fig. 10. Model for the noise study.

SpectreRF. The results show a gain of the second stage and the AB class output stage equal to 79 dB and 33 dB, respectively. These values, together with an 6 extra dB granted by the CDS z -transfer function, yield to a simulated effective 168-dB open loop DC gain.

A. Noise Study

Having a highpass filter $(1 - z^{-1})$ in the preamplification stage A_1 significantly reduces the $1/f$ noise. However, since successive samples are uncorrelated, the white term increases by 3 dB. The signal, instead, augments by 6 dB thanks to the $(1 + z^{-1})$ processing function. The result is a 3 dB increase in the signal-to-noise ratio (SNR). Moreover, as verified shortly, the scheme minimizes the input referred white noise at the cost of a slight reduction of the DC gain.

Consider Fig. 10 showing that the input referred noise spectrum, $v_{n,in}^2$, is amplified by the bandpass response of A_1 , giving a coloured bandpass spectrum. Then, the CDS sampling folds it to produce the result, shown in Fig. 9, substantially flat over the entire Nyquist interval. Only in the last decade it increases by about 2 dB. This noise is superposed to the kT/C noise and passed through the $(1 - z^{-1})$ filter. Since the signal is amplified by the gain at the chopping frequency, the noise spectrum referred to input is the noise power divided by $A_1^2(f_{\text{chop}})$.

The response of A_1 , shown in Fig. 9, can be approximated with two zeros at f_z , two poles at f_{p1} , and a third pole at f_{p2}

$$\begin{aligned} |A_1(f)|^2 &= A_1(0)^2 \frac{[1 + (f/f_z)^2]^2}{[1 + (f/f_{p1})^2]^2 [1 + (f/f_{p2})^2]} \\ &= A_1(0)^2 \frac{(1 + ax^2)^2}{(1 + bx^2)^2 (1 + x^2)} \end{aligned} \quad (6)$$

being $x = f/f_{p2}$, $a = f_{p2}/f_z$, and $b = f_{p2}/f_{p1}$, respectively.

The coloured spectrum at the output of A_1 becomes

$$v_{n,A_1}^2 = v_{n,in}^2 |A_1(f)|^2. \quad (7)$$

Its integral over the infinite frequency yields

$$\begin{aligned} V_{n,A_1}^2 &= f_{p2} v_{n,in}^2 A_1^2(0) \int_0^\infty \frac{(1 + ax^2)^2}{(1 + bx^2)^2 (1 + x^2)} dx \\ &= f_{p2} v_{n,in}^2 A_1^2(0) \frac{\pi}{2} f(a, b) \end{aligned} \quad (8)$$

where $f(a, b)$, assuming that $a \gg b$ ($f_z \ll f_{p1}$), the explicit solution of (8), [21], is

$$f(a, b) \approx \frac{a^2(1 - 3b) + 2ab(b + 1) + 2a^2b^{3/2}}{2b^{3/2}(b - 1)^2} \quad (9)$$

Fig. 11. Simulated input noise density as a function of the chopper frequency.

Therefore, the overall noise density is approximately

$$v_{n,CDS}^2 = 2 \frac{V_{n,A1}^2 + \gamma kT/C_{CDS}}{f_{chop}} \quad (10)$$

where γ accounts for the multiple capacitances of the CDS block.

The input referred noise spectrum becomes

$$v_{n,tot}^2 = \frac{v_{n,CDS}^2}{A_1^2(f_{chop})}. \quad (11)$$

The above study provides guidelines for the choice of the capacitor values in the CDS block and the A_1 frequency response. The used bandpass response of Fig. 9 shows an evident benefit because the noise spectrum is rejected at low frequency. Therefore, we expect better performance with respect to a single-pole response. The choice of zeros and poles is a tradeoff between gain at the chopping frequency and noise performance. For 500-kHz chopping, we choose $f_{p1} = 340$ kHz and $f_{p2} = 360$ kHz. The obtained peak gain is $A_{1,peak} = 420$. Using (8) and (9) $V_{n,A1}^2$ becomes $f_{p2}v_{n,in}^2 A_{1,peak}^2 0.63$, denoting a noise reduction of $\pi/(2 \cdot 0.63)$ with respect to the single dominant pole response of a conventional amplifier. $V_{n,A1}^2$ gives rise to an input referred noise divided by $f_{chop} A_1^2(f_{chop})$.

Fig. 11 shows the expected and the transistor level simulated input noise density as a function of chopping frequency. The noise drops significantly in the rising edge of $A_1(f)$. After the peak, the increase of f_{chop} is almost compensated by the reduction of gain. The optimum is around $f_{chop} = 500$ kHz. Since the gain at 500 kHz is about 3 dB below the peak, the resulting DC gain is only 3 dB less than the maximum achievable. Notice that the peak of the gain whose value is controlled by changing the bias current depends on the design. The above study shows that the optimal chopping frequency is about 50% higher than the peak frequency.

The periodic steady-state and periodic noise computer simulations at transistor level verify the above model calculations at various chopping frequencies. At 500 kHz the expected input noise is $35.6 \text{ nV}/\sqrt{\text{Hz}}$.

Fig. 12. Chip microphotograph.

The value of capacitances used in the CDS are not critical because their kT/C noise power is divided by $A_1^2(f_{chop})$ when referred to input. This design uses $C_{cds} = 500 \text{ fF}$ and $C_s = 1 \text{ pF}$.

VI. MEASUREMENT RESULTS

The fabricated chopper CDS amplifier has been extensively tested. Fig. 12 shows its microphotograph. The total occupied area is $1.21 \text{ mm} \times 0.95 \text{ mm}$, including the pads ring. The supply voltage can range from 1.8 V to 5 V with a common mode input range of 0–5 V. The analog quiescent current is $12.8 \mu\text{A}$. The current needed by the internal ring oscillator and logic for a chopping frequency of 500 kHz is $1.6 \mu\text{A}$.

Fig. 13 shows the Bode diagram of the amplifier, measured from 100 Hz to 1 MHz. As expected, the phase margin at 20-dB gain is about 71° . The corresponding frequency is approximately 26 kHz. Therefore, the extrapolated GBW is about 260 kHz. Since the CDS delay is $1 \mu\text{s}$, it is negligible compared to $1/(2\pi f_B)$ (f_B is the signal band). The DC gain is 168 dB with dominant pole, given by the second amplification stage, at 1.1 mHz. The lowpass action of the second stage makes continuous-time the output waveform.

The measured input noise density spectrum of Fig. 14 shows a low-frequency level of $37 \text{ nV}/\sqrt{\text{Hz}}$ without flicker noise. The result almost matches the periodic steady-state simulation results and periodic noise analyses made with SpectreRF. The spectrum is flat up to the limit of the test equipment (10 Hz) and does not show any tone at the chopping frequency (500 kHz) or its multiples. The noise measurements are made with a closed-loop gain equal to 1027. Tests performed with closed-loop gains as low as 10 do not show tones above the noise floor at chopping frequency.

Noise flatness in the 0.1–10 Hz interval (below the spectrum analyzer bandwidth) has been verified by time domain measurement, as illustrated in Fig. 15. The peak-to-peak voltage is $0.8 \mu\text{V}$. Fig. 16 shows a low-frequency periodic noise simulation. The simulated corner frequency is 20 mHz, higher than [7], but enough for the expected applications.

The offset voltage measured over the 44 available samples gives the population distribution of Fig. 17. The obtained variance is about $2 \mu\text{V}$. The result is close to the simulation values and almost corresponds to the expected contribution of the second stage of the architecture. The measures at different

Fig. 13. Measured amplifier Bode diagram.

Fig. 14. Measured input noise spectrum with 1027 closed-loop gain.

Fig. 15. Low-frequency noise measurement.

temperatures show that the chopper CDS amplifier operates properly in the -40°C to 125°C range with a temperature dependence of offset better than $0.03\ \mu\text{V}/^{\circ}\text{C}$.

Fig. 18 shows the response of the amplifier (channel 4) with 192-mV input step at about 500 Hz (channel 2, AC coupled). The power supply is 5 V and the amplifier gain is about 10.

Fig. 16. Low-frequency periodic noise simulation.

Fig. 17. Measured offset voltage distribution.

Fig. 18. Measured input step response.

Table I summarizes the performance and compares this circuit with other state-of-the-art amplifiers. The measured input noise density and the low current consumption give a noise efficiency factor (NEF), [22], defined as

$$\text{NEF} = v_{n,in} \sqrt{\frac{2I_{tot}}{\pi U_T 4kT}} \quad (12)$$

equal to 5.5.

TABLE I
COMPARISON WITH STATE-OF-THE-ART AMPLIFIERS

	This Work	[8]	[6]	[18]
Year of Publication	2010	2010	2006	2005
Process	0.18–0.5 μm CMOS	0.7 μm CMOS	0.3–0.6 μm CMOS	0.18 μm CMOS
Chopping Frequency	500 kHz	30 kHz	125 kHz	1 MHz
Autozero Frequency	-	-	-	<0.001 kHz
Input Noise Density at DC	37 nV/ $\sqrt{\text{Hz}}$	10.5 nV/ $\sqrt{\text{Hz}}$	55 nV/ $\sqrt{\text{Hz}}$	50 nV/ $\sqrt{\text{Hz}}$
Offset Voltage Standard Deviation	1.94 μV	1 μV	3 μV	-
Supply Current	14.4 μA	143 μA	17 μA	500 μA
GBW	260 kHz (extrapolated)	1.8 MHz	350 kHz	100 MHz
Offset Temperature Dependence	<0.03 $\mu\text{V}/^\circ\text{C}$	-	0.02 $\mu\text{V}/^\circ\text{C}$	-
CMRR	124 dB	136 dB	-	38 dB
PSRR	120 dB	-	-	66 dB
Chip Area	1.14 mm ²	1.8 mm ²	0.7 mm ²	0.88 mm ²

VII. CONCLUSION

Low-power spur-free amplification with offset cancellation is obtained by the combined action of input chopping and CDS. The use of a bandpass input amplifier avoids saturation even if the stage is DC open loop. Moreover, the same stage reduces the low-frequency noise spectrum with respect to conventional low-pass counterparts. The proposed circuit, integrated in a mixed 0.18–0.5- μm CMOS technology, operates with 500-kHz chopping frequency. The overall current consumption is 14.4 μA with 320-pF load. The supply voltage of the rail-to-rail input scheme can range from 1.8 V to 5 V. The standard deviation of offset, obtained over the 44 available samples, is 2 μV . The offset temperature coefficient is better than 30 nV/ $^\circ\text{C}$ in the range from -40°C to 125°C . The low-frequency input referred noise density is 37 nV/ $\sqrt{\text{Hz}}$ without noticeable flicker noise.

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