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Time-Interleaved Sigma-Delta Modulator Using Output Prediction Scheme

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Abstract—A time-interleaved sigma-delta modulator using the output prediction scheme is proposed. This approach uses only one integrator channel along with incomplete integrator output terms to eliminate the quantizer domino which is a key limit for practical circuit implementation of conventional time-interleaved sigma-delta modulators. In addition, channel mismatch effects due to mismatch within multiple integrator feedback paths can be reduced by optimizing the feedback path. An equivalent two-channel time-interleaved version of the conventional second-order sigma-delta modulator is realized to verify the proposed method.

Index Terms—Channel mismatch, incomplete integrator outputs, output prediction, quantizer domino, sigma-delta modulators, time-interleaved.

I. INTRODUCTION

SIGMA-DELTA ($\Sigma\Delta$) techniques have been widely used for low-bandwidth and high-resolution applications owing to the oversampling and noise shaping feature [1], [2]. However, $\Sigma\Delta$ applications are being extended to new telecommunication areas, which typically require megahertz-range signal bandwidth with a sampling clock near 100 MHz [3]. With high sampling clocks, the CMOS implementation of $\Sigma\Delta$ modulators is problematic due to the high-frequency limitations of the opamps and sampling switches.

Time-interleaved (TI) $\Sigma\Delta$ modulators are an attractive solution for high-speed applications, since the oversampling rate (OSR) can be increased without speeding up the analog blocks [4]–[7]. However, the recursive operation of $\Sigma\Delta$ modulators, which is not used in Nyquist rate interleaved converters [8], complicates the direct conversion into their equivalent TI structures [6]. Among the TI concepts for $\Sigma\Delta$ modulators, the block digital filtering [4], [5] and the extended hardware reduction approach [6], [7] conceptually works well, but quantizer domino and channel mismatch effects limit the circuit implementation. Quantizer domino occurs when a certain quantizer output is connected to another quantizer input via an analog block without passing through a delay element. This situation is unavoidable in M -channel TI $\Sigma\Delta$ modulators, when M consecutive modulator outputs are simultaneously generated by M quantizers. In

the block digital filtering approach, quantizer domino can only be prevented for two-channel structures by using a double-sampling switched-capacitor (SC) scheme [5].

This brief presents a predictive TI scheme for $\Sigma\Delta$ modulators that is completely free of the quantizer domino. Furthermore, simulation results show that the proposed two-channel TI second order $\Sigma\Delta$ modulator is less sensitive to channel mismatch effects than other two-channel TI $\Sigma\Delta$ modulators.

II. PROPOSED TI $\Sigma\Delta$ MODULATOR

A. TI Scheme Overview

We describe the proposed TI scheme through a time-domain study of the conventional $\Sigma\Delta$ modulator and the equivalent M -channel TI structure. Fig. 1(a) shows a general L th order $\Sigma\Delta$ modulator with distributed feedback and feedforward branches [1], where a_i and b_i are constant coefficients. Each integration symbol represents either a delayed or nondelayed sampled-date integrator, except for the L th integrator which is a delayed integrator. The modulator output y is the quantized version of the L th integrator output p_L . Since the subsystem enclosed within the dotted line of Fig. 1(a) is linear with input x , feedback y , and output p_L , the future outputs of the L th integrator can be described as

$$p_L(n+j) = p_{zi}(n+j) + p_{x,zs}(n+j) + p_{y,zs}(n+j), \quad \text{for } j > 0 \quad (1)$$

where n and j are integers. Here p_{zi} is the zero input response or natural response, and $p_{x,zs}$ and $p_{y,zs}$ are the zero state response or forced response of the subsystem with respect to the input x and the feedback y . Assuming $p_L(n)$ is the initial output, the $M-1$ consecutive time slot outputs of the L th integrator can be written as

$$p_L(n+j) = p_L(n) + \sum_{i=1}^{L-1} h_i(j)p_i(n) + \sum_{i=0}^{j-1} s(j-i)x(n+i) - \sum_{i=0}^{j-1} f(j-i)y(n+i), \quad \text{for } j = 1, \dots, M-1 \quad (2)$$

where the first two terms correspond to the zero input response, and the remaining two terms represent the zero state response with x and y applied from time slot n . In addition, h_i is a coefficient due to the recursive operation of the n th time slot integrator outputs $p_i(n)$ for $i = 1, \dots, L$. Moreover, s and f are the

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Fig. 1. L th order $\Sigma\Delta$ modulators with distributed feedback and feedforward branches. (a) Conventional and (b) proposed M -channel TI.

impulse response determined at the L th integrator by the input x and feedback y , respectively.

Since the TI operation requires the future outputs of p_L , it is convenient to redefine each variable used in (2) such that it is assigned to the j th channel of the TI modulator as

$$x_j(n') = x[Mr + j], \quad \text{for } j = 1, \dots, M \quad (3a)$$

$$y_j(n') = y[Mr + j], \quad \text{for } j = 1, \dots, M \quad (3b)$$

$$p_{i1}(n') = p_i[Mr + 1], \quad \text{for } i = 1, \dots, L \quad (3c)$$

where r is an integer for $r \geq 0$, n' is the decimated timing of the TI modulator, and $p_{i1}(n')$ is the zero input initial condition of the i th integrator, which corresponds to the n' th time slot integrator output. Using (3a)–(3c), (2) can be rewritten as

$$\begin{aligned} p_{Lj}(n') &= p_{L1}(n') + \sum_{i=1}^{L-1} h_i(j-1)p_{i1}(n') \\ &+ \sum_{i=1}^{j-1} s(j-i)x_i(n') - \sum_{i=1}^{j-1} f(j-i)y_i(n'), \\ &\text{for } j = 2, \dots, M. \end{aligned} \quad (4)$$

To generate the p_{Lj} terms, it is necessary to know the future signals $x[Mr + j]$ and $y[Mr + j]$ for $j = 2, \dots, M$. For the inputs x , using an M -clock sample-and-hold version x_{sd} instead of x permits the lack of the future inputs: $x_{sd}[Mr + j] = x[Mr]$. Alternatively, the future values of x can be determined by using an $(M-1)$ -clock delayed version of x , that is $x_d[Mr + j] = x[M(r-1) + j]$. Unfortunately, using the future feedback terms $y[Mr + j]$ for $j > 1$ directly leads to quantizer domino—only $y_1(n')$ can be determined by quantizing the initial condition $p_{L1}(n')$. Since it is not possible

to generate the future terms of $p_{Lj}(n')$ for $j > 1$, let us consider the incomplete integrator outputs $p_{Lj}^*(n')$, defined as

$$\begin{aligned} p_{Lj}^*(n') &= p_{L1}(n') + \sum_{i=1}^{L-1} h_i(j-1)p_{i1}(n') \\ &+ \sum_{i=1}^{j-1} s(j-i)x_i(n'), \quad \text{for } j = 2, \dots, M. \end{aligned} \quad (5)$$

Furthermore, using (4), (5) can be rewritten as

$$p_{Lj}^*(n') = p_{Lj}(n') + \sum_{i=1}^{j-1} f(j-i)y_i(n'), \quad \text{for } j = 2, \dots, M. \quad (6)$$

Since the quantization of $p_{Lj}(n')$ leads to the modulator output $y_j(n')$, the quantization of (6) yields

$$\begin{aligned} y_j^*(n') + \varepsilon_j(n') &= y_j(n') + \varepsilon_j(n') + \sum_{i=1}^{j-1} f(j-i)y_i(n'), \\ &\text{for } j = 2, \dots, M \end{aligned} \quad (7)$$

where $\varepsilon_j(n')$ is the quantization error which affects the SNR of the TI $\Sigma\Delta$ modulator by contributing to the quantization noise power. Finally, (7) leads to

$$y_j^*(n') = y_j(n') + \sum_{i=1}^{j-1} f(j-i)y_i(n'), \quad \text{for } j = 2, \dots, M. \quad (8)$$

Therefore, the complete output set $y_j(n')$ for $j = 1, \dots, M$ can be obtained by a suitable digital processing of the complete output $y_1(n')$ and incomplete outputs $y_j^*(n')$ for $j = 2, \dots, M$. Here, the required digital processing does not cause quantizer domino. However, the quantizers which generate the $y_j^*(n')$

Fig. 3. SC implementation of the proposed two-channel TI second-order $\Sigma\Delta$ modulator.

Fig. 4. Output spectra with the same internal clock frequency.

Fig. 5. Output spectra of two-channel TI second-order $\Sigma\Delta$ modulators with 0.5% channel mismatch.

Channel mismatch effect is a potential drawback for multichannel TI $\Sigma\Delta$ modulators. With channel mismatch, the in-band noise level of the M -channel TI $\Sigma\Delta$ modulator will increase, since the spectral components around $2\pi i/M$ for $i = 1, \dots, M-1$, will be folded back into the signal band [5], [6]. Fig. 5 shows the output spectra of three different two-channel TI second-order $\Sigma\Delta$ modulators with 0.5% channel mismatch. Here, TI-(I) refers to the block digital filtering scheme with the k -factor technique [5], and TI-(II) denotes the extended hardware simplified version [6]. Results show the SNDR degradation of the proposed TI modulator is around 2 dB with 0.5% channel mismatch, which is less than the other two-channel TI structures. This is mainly due to the single feedback path of the first integrator, since the feedback terms of the first integrator will be affected by an identical error, thus reducing the spur around f_s . As expected, the SNDR

degradation due to the mismatch between the two feedback paths of the second integrator was negligible.

IV. CONCLUSION

In this brief, we have presented a new TI scheme for $\Sigma\Delta$ modulators. The proposed method is able to eliminate the quantizer domino within the TI $\Sigma\Delta$ modulator, regardless of the channel count. The reduced channel mismatch effect is an extra benefit of the proposed approach which is enabled by using a single integrator channel with an optimized feedback path. The SNDR degradation of the proposed two-channel TI second-order $\Sigma\Delta$ modulator respect to channel mismatch effect was relatively less compared to other two-channel TI $\Sigma\Delta$ modulators. Finally, the proposed TI scheme can be even practical for circuit implementation of TI $\Sigma\Delta$ modulators with more than two channels.

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