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Layout of Analog CMOS Integrated Circuit

Part 3

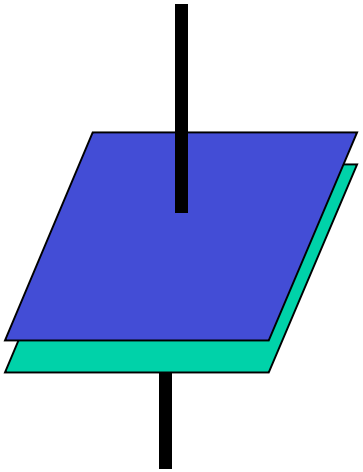
Passive components: Resistors, Capacitors

Outline

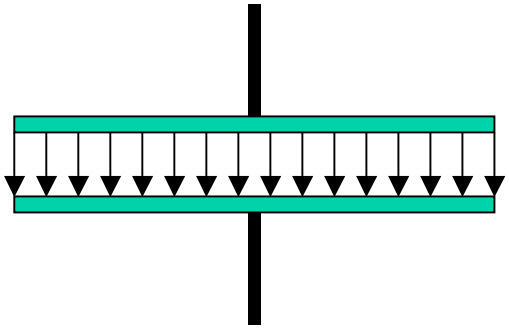
- Introduction
- Process and Overview Topics
- Transistors and Basic Cells Layout
- Passive components: Resistors, Capacitors
- System level Mixed-signal Layout

Integrated Capacitors

Capacitors in IC are parallel plate capacitors



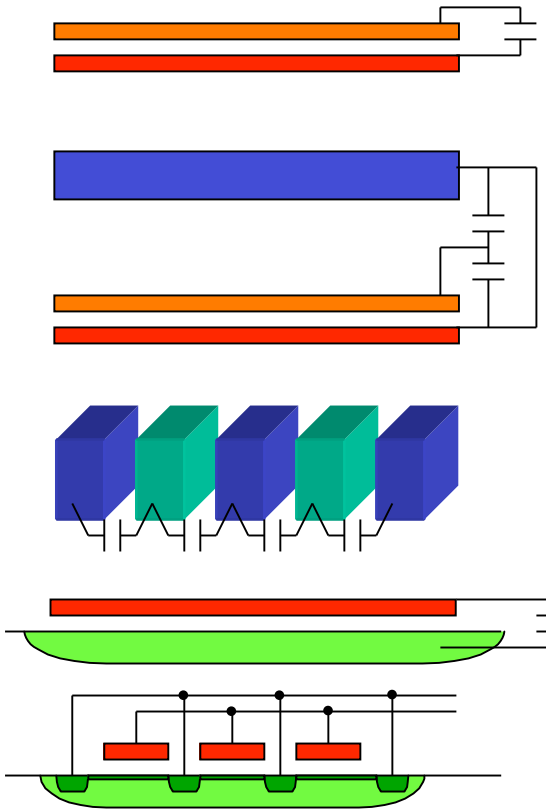
No fringing effect →



$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$$

Material	Rel. Permittivity	Diel. Strength
SiO_2 Dry Oxide	3.9	11 V/nm
SiO_2 Plasma	4.9	3-6 V/nm
Si_3N_4 LPCVD	6-7	10 V/nm
Si_3N_4 Plasma	6-9	5 V/nm

Types of Integrated Capacitors



Poly-poly

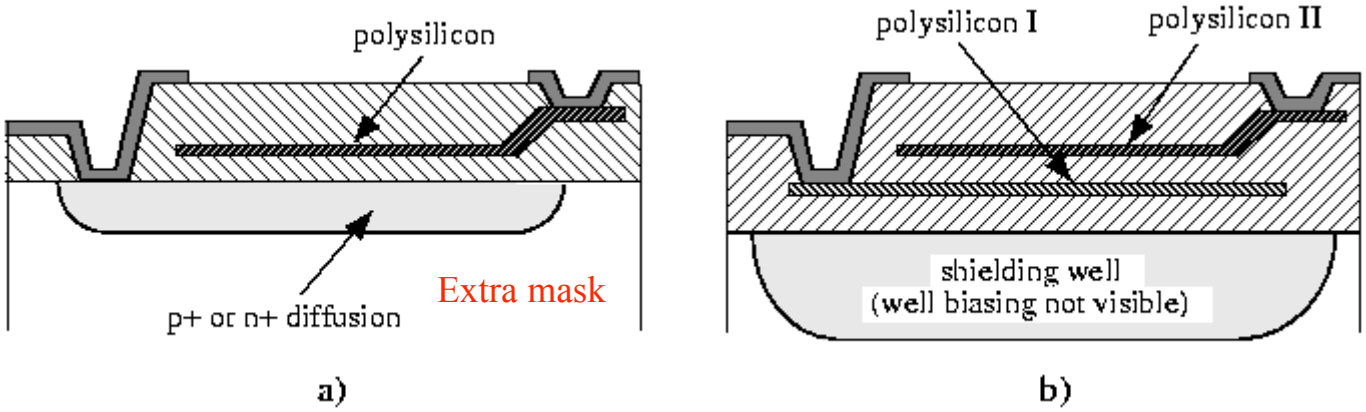
Sandwich

Lateral plates
(flux capacitor)

Poly- diffusion

Poly-channel

Features of Integrated Capacitors



Electrodes : metal; polysilicon; diffusion

Insulator : silicon oxide; polysilicon oxide; CVD oxide

$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$$

$$\left(\frac{\Delta C}{C}\right)^2 = \left(\frac{\Delta \varepsilon_r}{\varepsilon_r}\right)^2 + \left(\frac{\Delta t_{ox}}{t_{ox}}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2$$

Factor affecting accuracy

$\left(\frac{\Delta\varepsilon_r}{\varepsilon_r}\right)$

- Oxide damage
- Impurities
- Bias condition
- Bias history (for CVD)
- Stress
- Temperature

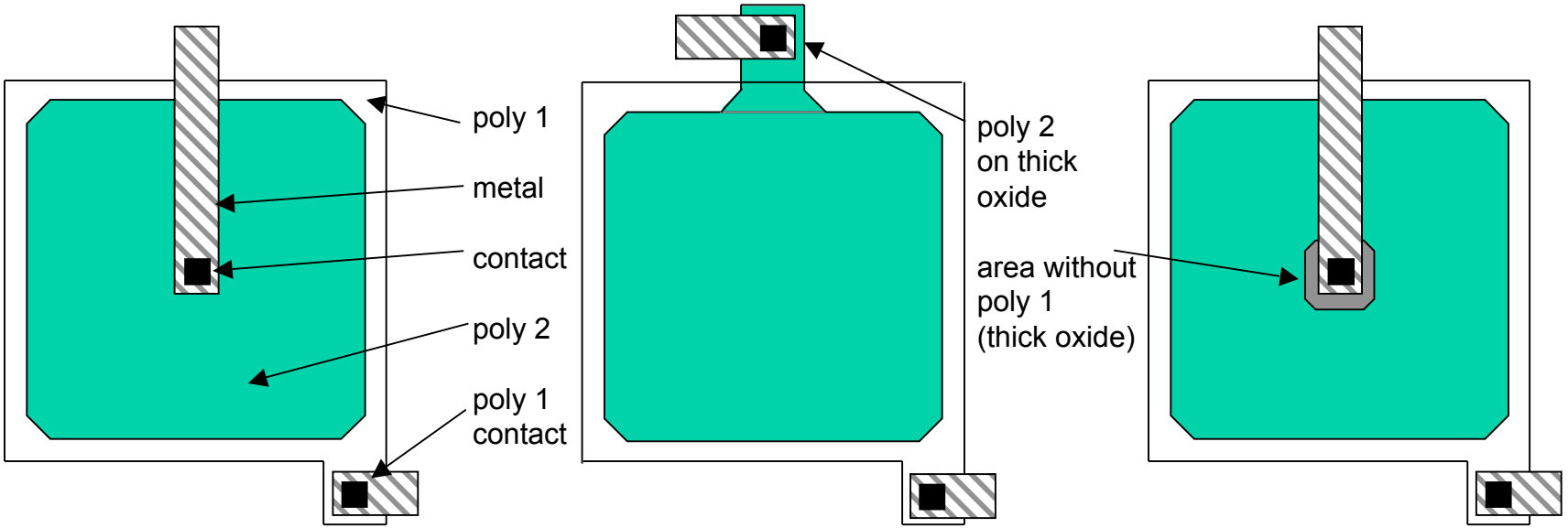
$\left(\frac{\Delta t_{ox}}{t_{ox}}\right)$

- Grow rate
- Poly grain size

$\left(\frac{\Delta L}{L}\right);\left(\frac{\Delta W}{W}\right)$

- Etching
- Alignment

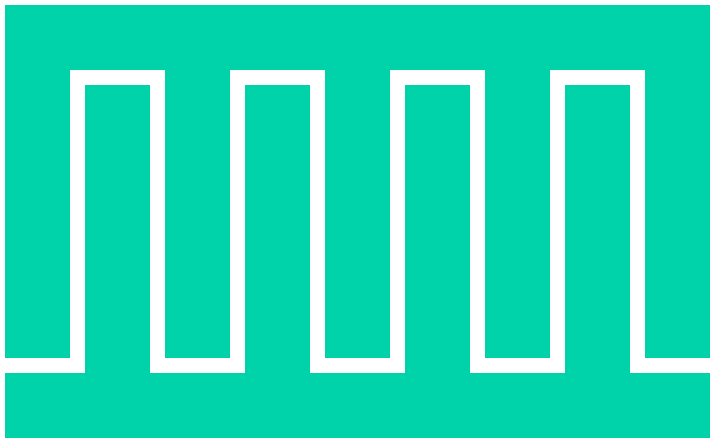
Layout of Capacitors



To achieve good matching :

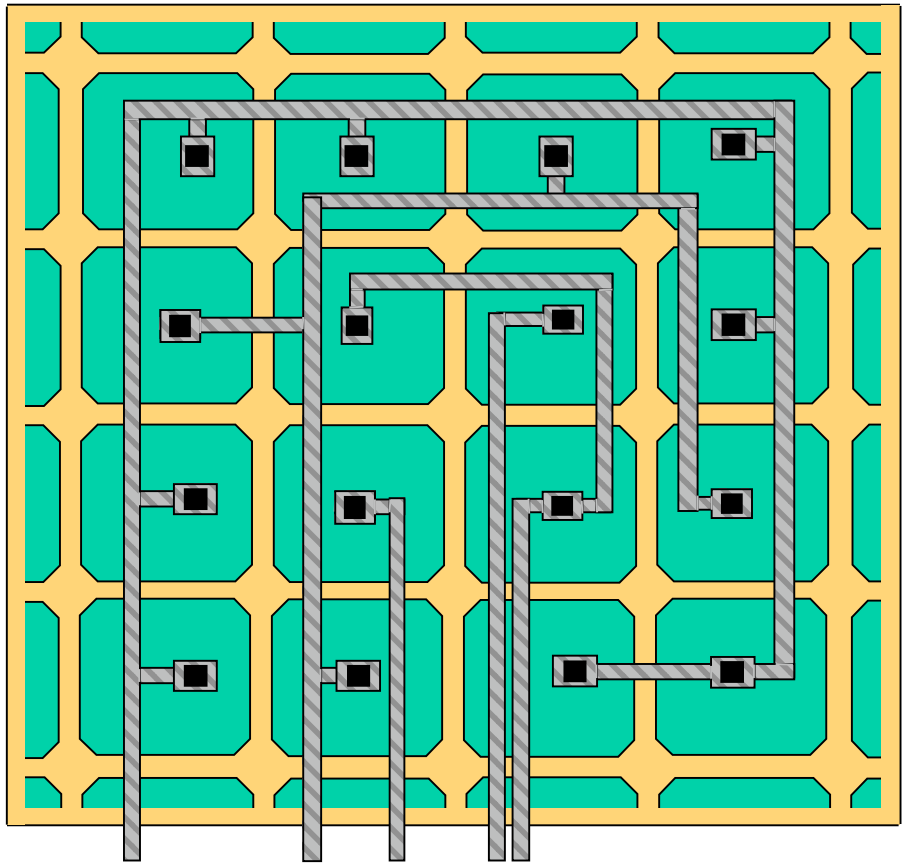
- Use of unity capacitors connected in parallel
- Use W = L fairly large

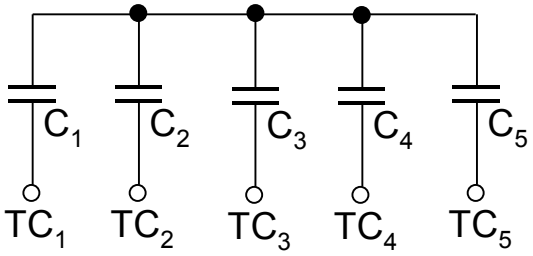
Flux Capacitor Layout



- Use of the same metal layer
- Exploit the lateral flux
- The parasitic capacitance plate -substrate is low because the metal sits on thick oxide
- Use thick metal layers
- Maximize the perimeter (use of fractals)
- Very good matching!

Common Centroid Structures





$C_2 = C_1$
$C_3 = 2C_1$
$C_4 = 4C_1$
$C_5 = 8C_1$

Matching of Capacitors

Matching accuracy is better than matched resistors, because :

- $\left(\frac{\Delta\varepsilon_r}{\varepsilon_r}\right) << \left(\frac{\Delta\bar{\rho}}{\bar{\rho}}\right)$
- $\left(\frac{\Delta W}{W}\right)_{cap} < \left(\frac{\Delta W}{W}\right)_{res}$ (because the capacitors are square)
- $\left(\frac{\Delta t_{ox}}{t_{ox}}\right) < \left(\frac{\Delta x_j}{x_j}\right)$

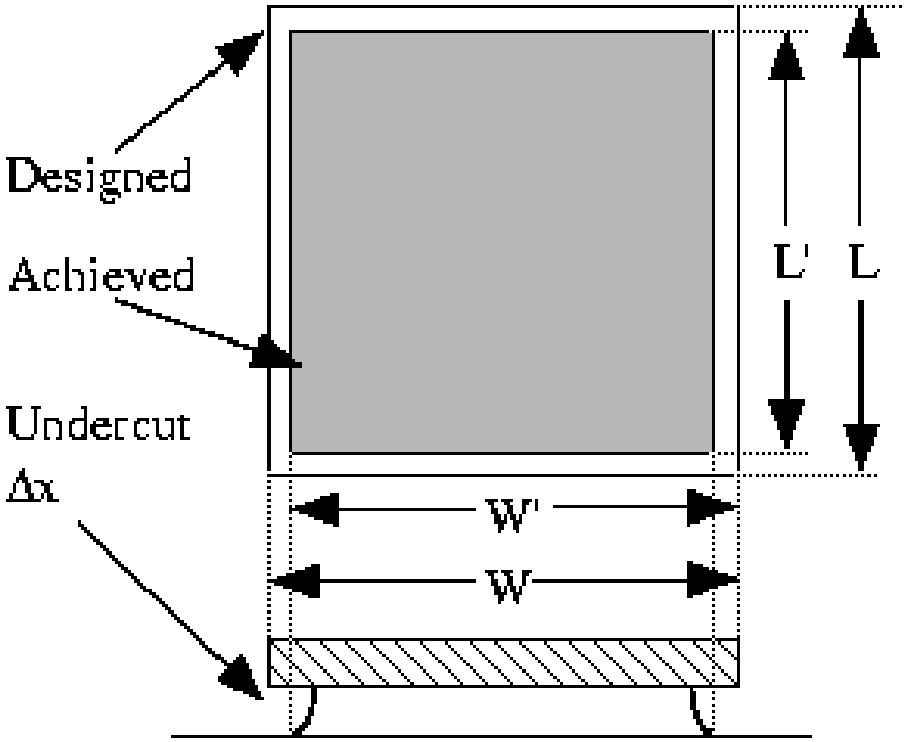
Undercut Effect

W’ = W - 2x
L’ = L - 2x

Effective area :

A’ = W’L’ = WL - 2(L + W)x
A’= A - Px

The undercut effect gives the same proportional reduction if the perimeter-area ratio is kept constant

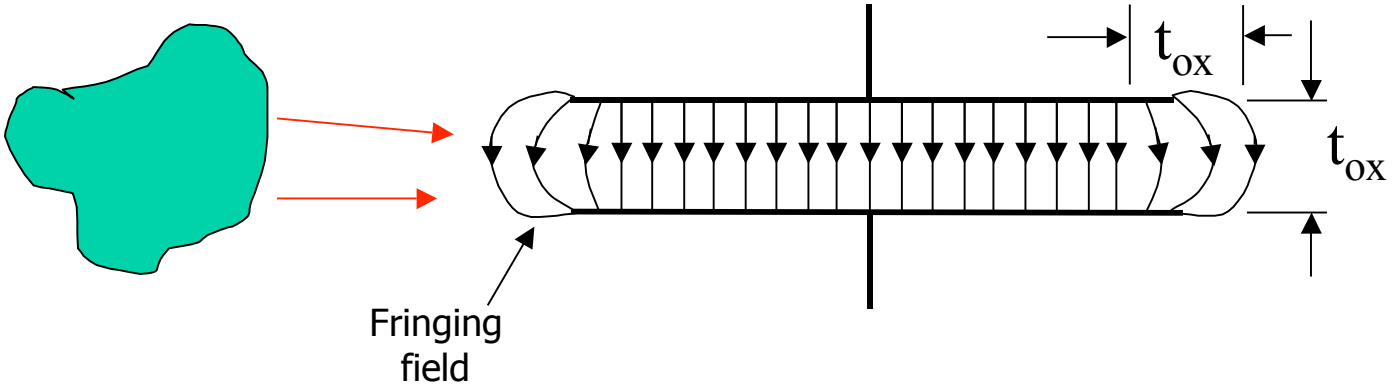


Matched Capacitors: Exercise

- Layout the following three capacitors
  - C_1= 0.95 pF
  - C_2=1.24 pF
  - C_3= 1.37 pF
  - The absolute accuracy is not important. What matter is the capacitance ratios.

Fringing Effect

- Equation $C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$ is an approximation



$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} (W - t_{ox})(L - t_{ox}) + C_{fring}$$

- Fringing depends on the boundary conditions

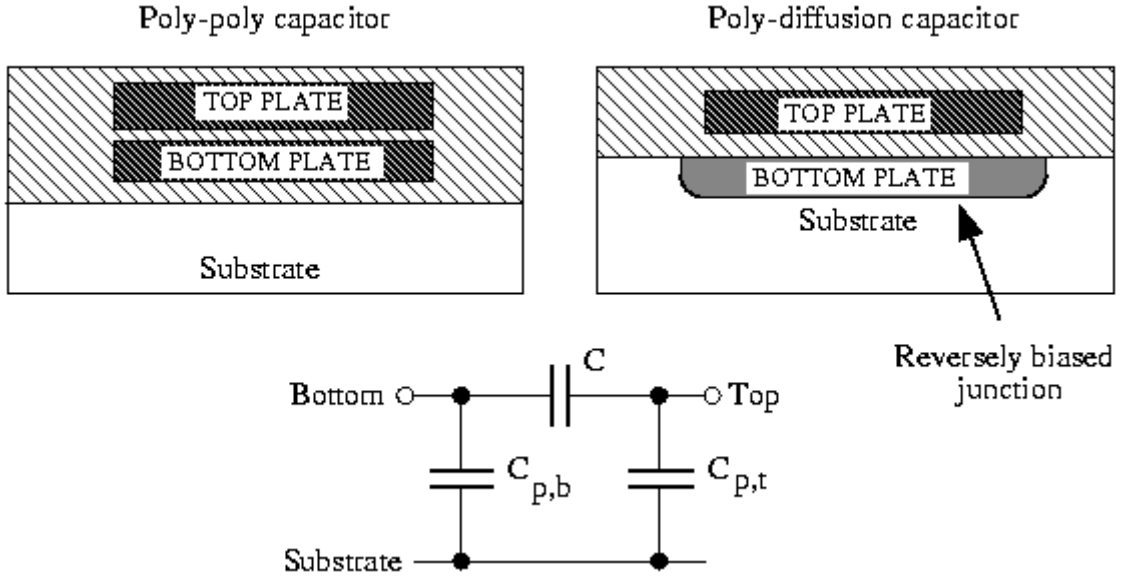
MOS Capacitors Features

Type	t_{ox} nm	Accuracy %	Temperature Coefficient ppm/°C	Voltage Coefficient ppm/V
poly - diff.	15 - 20	7 - 14	20 - 50	60 - 300
poly I - poly II	15 -25	6 - 12	20 - 50	40 - 200
metal - poly	500 - 700	6 - 12	50 - 100	40 - 200
metal - diff.	1200 - 1400	6 - 12	50 - 100	60 - 300
metal I - metal II	800 - 1200	6 - 12	50 - 100	40 – 200

Parasitic Capacitances

	diffusion	poly-poly or poly-metal
$C_{p,b}$	*0.05C*	*0.02 C*
$C_{p,t}$	*0.01C*	*0.005 C*

High impedance node connected to the top plate



Rules for Capacitor Matching

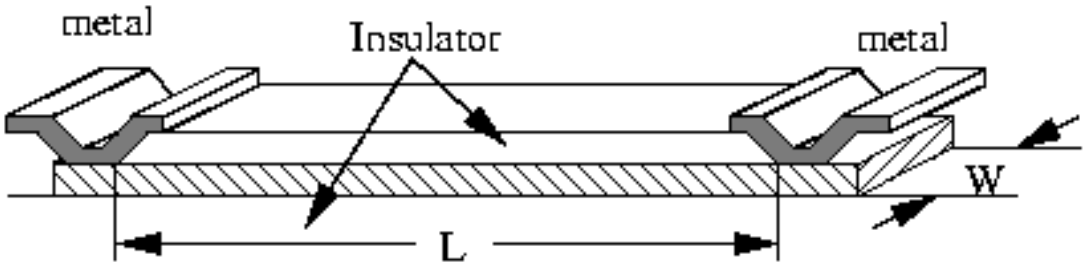
- Use identical geometries
- Use large unity capacitance (minimize fringing)
- Use common centroid arrangement
- Use dummy capacitors
- Use shielding
- Account for the connections' contribution
- Don't run connections over capacitor
- Place capacitor in low stress areas
- Place capacitors far from power devices

Integrated Capacitors

- Issues to remember
  - Use unit capacitors
  - Make bigger capacitors integer multiples of the unit capacitor
  - Use common centroid layout to match capacitors
  - Use multiple contacts to lower series resistance

Integrated Resistor Cross-section

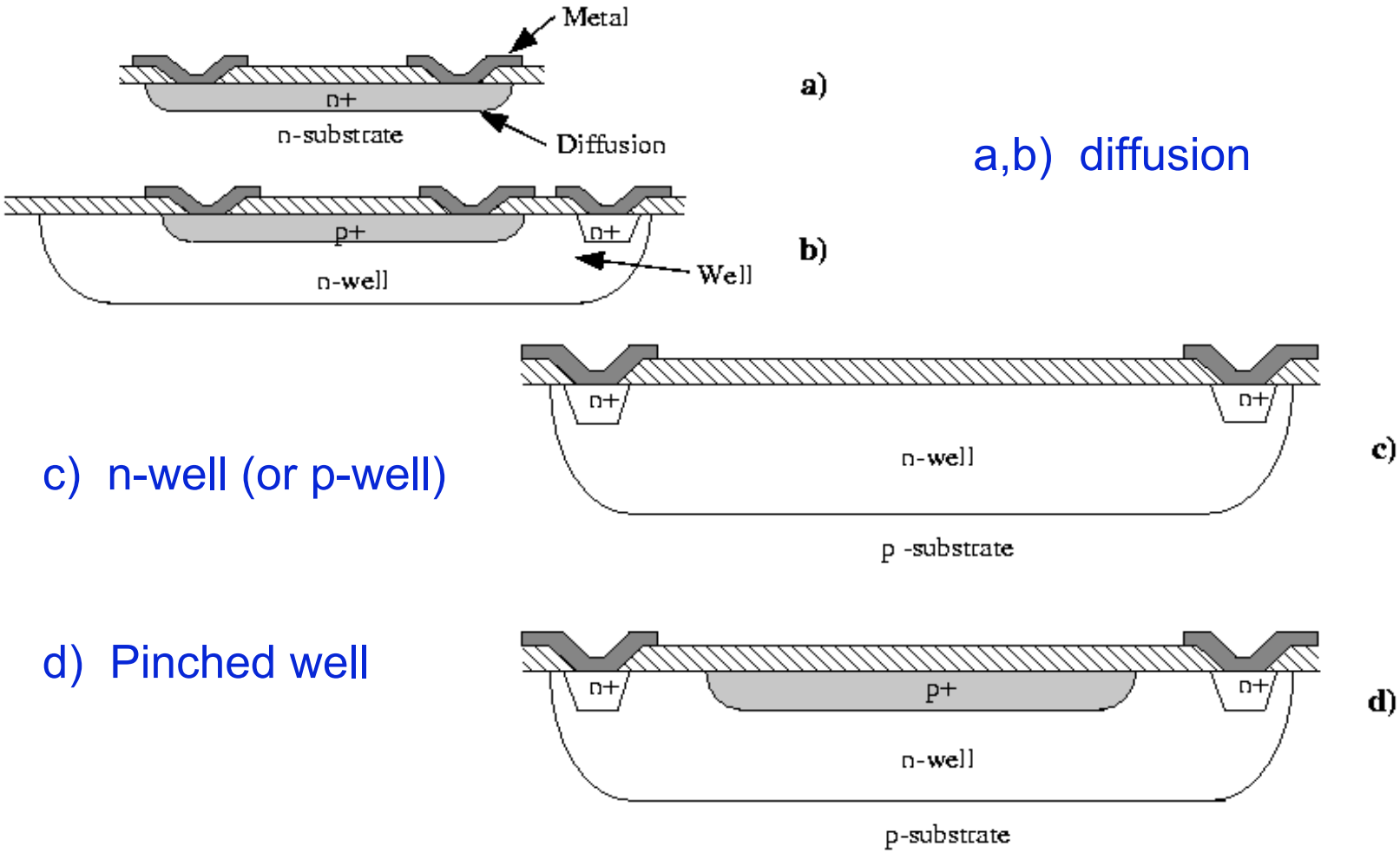
- A resistor is made of a strip of resistive layer.



$$R = 2R_{cont} + \frac{L}{W} R_{\square}$$

- The endings resistance can be significant!

Diffused Resistances

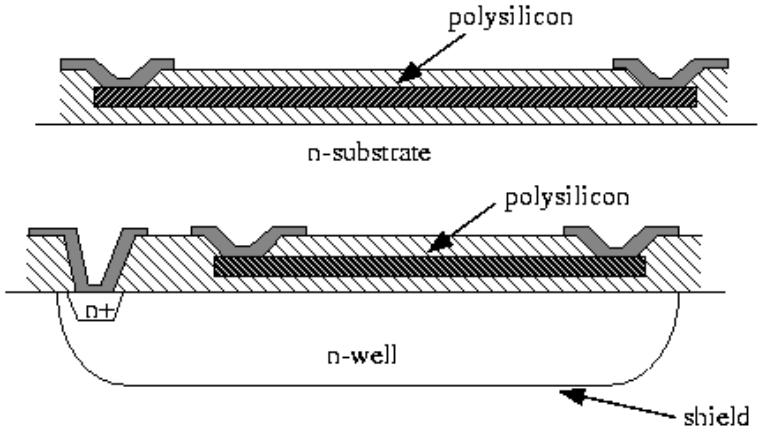


a,b) diffusion

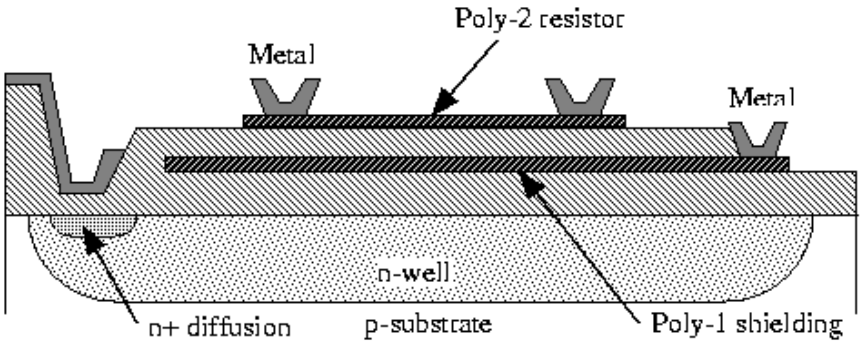
c) n-well (or p-well)

d) Pinched well

Polysilicon Resistances



g)



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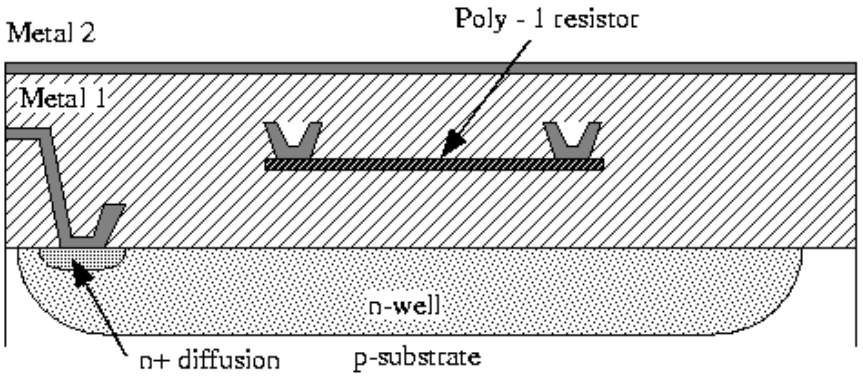
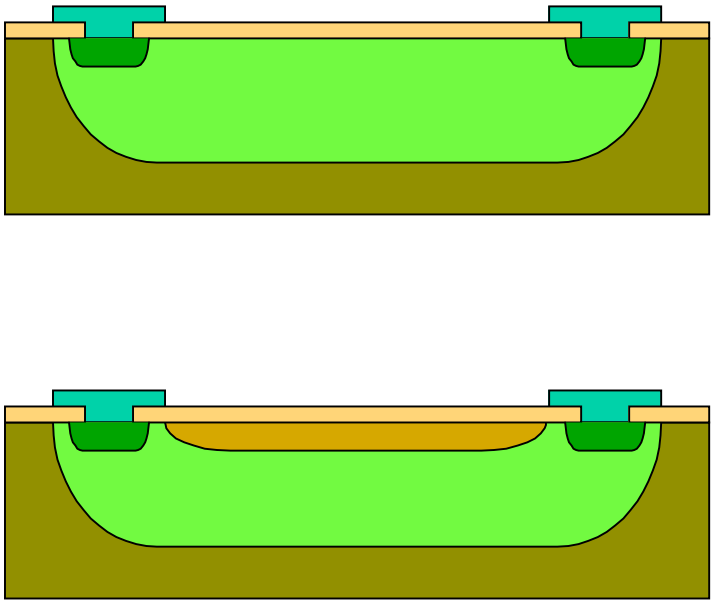


Conductive layers can be used to shield the conductor-oxide-conductor structure

Well or Pinched-well Resistors



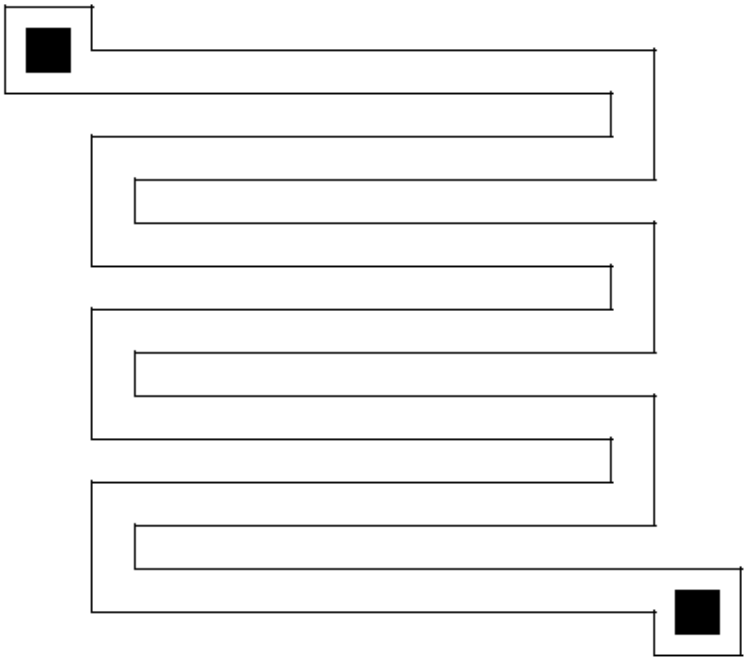
- Well layers have a large specific resistance
- but
- They have a large voltage and temperature coefficient
- They are weakly insulated from the surrounding
- Layers close to the surface contribute to the conductivity

Large Value Resistors

In order to have large value resistors :

- Use of long strips (large L/W)
- Use of layers with high sheet resistance (bad performances)

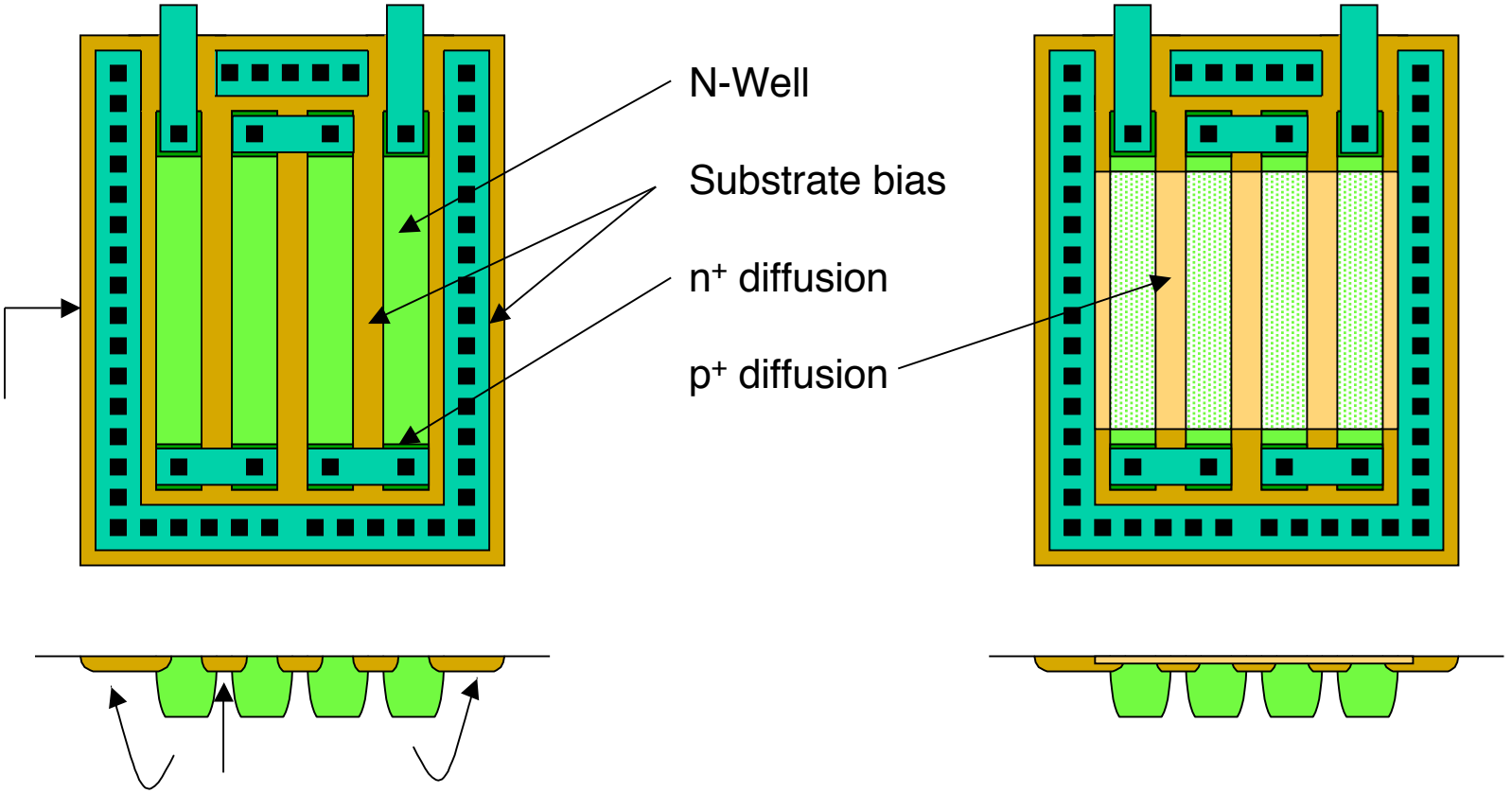
Layout : rectangular “snake”



(!!)
Resistance at the corners
Current flows in different directions

DON’T USE IT IN PRECISE APPLICATIONS!

Prevent Current Leakage!



Features of Resistors

Type of layer	Sheet Resistance Ω/0	Accuracy %	Temperature Coefficient ppm/°C	Voltage Coefficient ppm/V
n + diff	30 - 50	20 - 40	200 - 1K	50 - 300
p + diff	50 -150	20 - 40	200 - 1K	50 - 300
n - well	2K - 4K	15 - 30	5K	10K
p - well	3K - 6K	15 - 30	5K	10K
pinched n - well	6K - 10K	25 - 40	10K	20K
pinched p - well	9K - 13K	25 - 40	10K	20K
first poly	20 - 40	25 - 40	500 - 1500	20 - 200
second poly	15 - 40	25 - 40	500 - 1500	20 - 200

Resistor's Accuracy

$$R = \frac{L}{W} R_{\square} = \frac{L}{W} \cdot \frac{\bar{\rho}}{x_j}$$

If the parameter are statistically independent the standard deviation of the resistance is :

$$\left(\frac{\Delta R}{R}\right)^2 = \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2 + \left(\frac{\Delta \bar{\rho}}{\bar{\rho}}\right)^2 + \left(\frac{\Delta x_j}{x_j}\right)^2$$

Since in general L >> W $\left(\frac{\Delta L}{L}\right) << \left(\frac{\Delta W}{W}\right)$

Resistor's Accuracy (cont.)

$\left(\frac{\Delta\bar{\rho}}{\bar{\rho}}\right)$ for polysilicon resistors is larger than for diffused resistors.

(Polysilicon is composed of a conglomerate of independently oriented grain of crystalline silicon)

Accuracy :

Absolute accuracy is poor because of the large parameter drift

Ratio (or matching) accuracy is better because it depends on the local variation of parameters.

Factor Affecting Accuracy

$\left(\frac{\Delta\bar{\rho}}{\bar{\rho}}\right)$

- Polysilicon grain size
- Doping dose
- Crystal defects
- Stress
- Temperature

$\left(\frac{\Delta L}{L}\right);\left(\frac{\Delta W}{W}\right)$

- Etching
- Boundary
- Side diffusivity

$\left(\frac{\Delta x_j}{x_j}\right)$

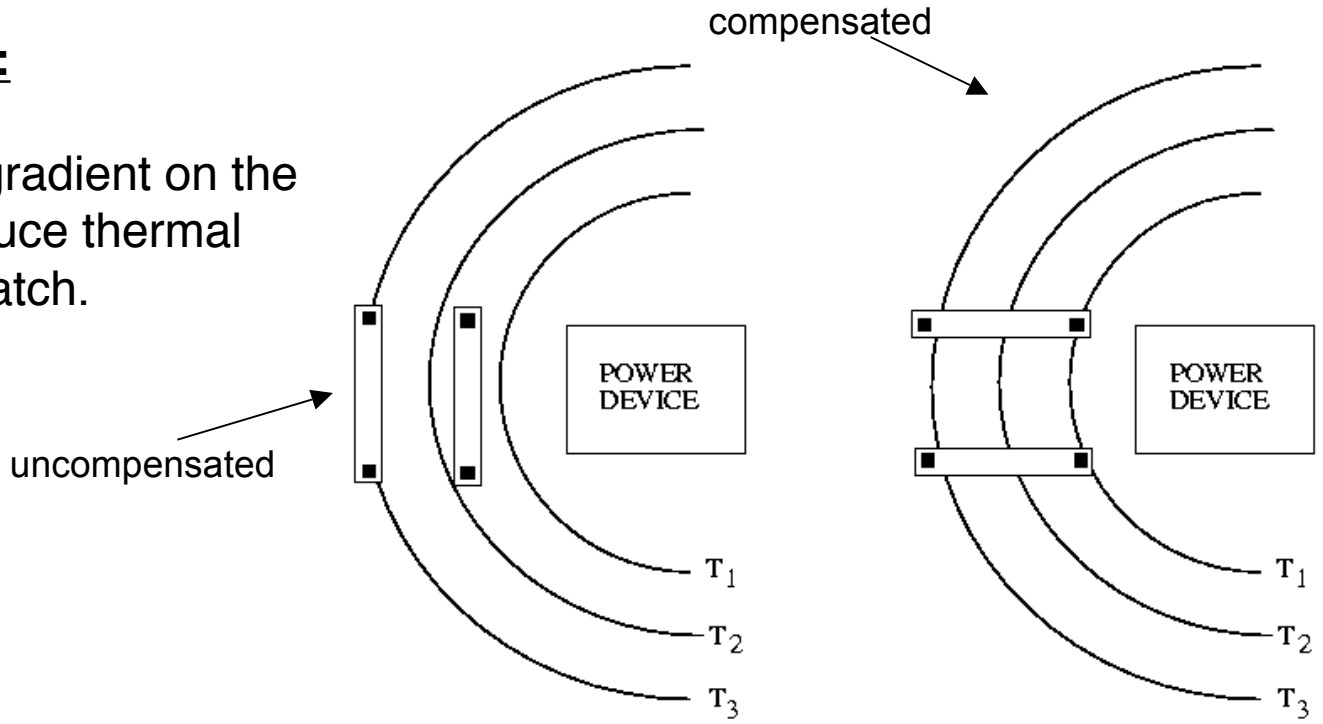
- Implant dose
- Side diffusivity
- Deposition rate

Other Elements

Plastic packages cause a large pressure on the die (= 800 Atm.). It determines a variation of the resistivity.
For <100> material the variation is unisotropic, so the minimum is get if the resistance have a 45° orientation.

Temperature :

Temperature gradient on the chip may produce thermal induced mismatch.

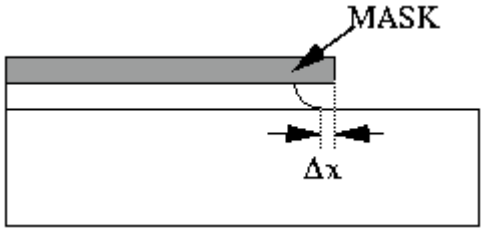


Effect of Etching

Wet etching : isotropic (undercut effect)

H_F for SiO_2 ; H_3PO_4 for Al

Δx for polysilicon may be 0.35 - 0.5 μ with standard deviation 0.02 μ.



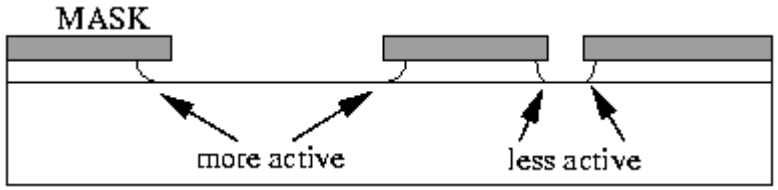
Reactive ion etching (R.I.E.)(plasma etching associated to “bombardment”) : unisotropic.

Δx for polysilicon is 0.2 μ with standard deviation 0.015 μ

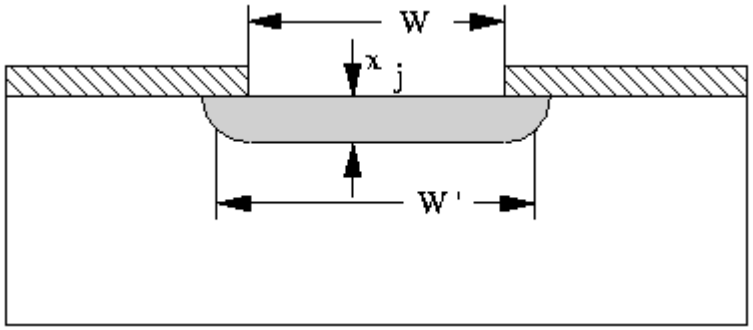
Boundary :

The etching depends on the boundary conditions

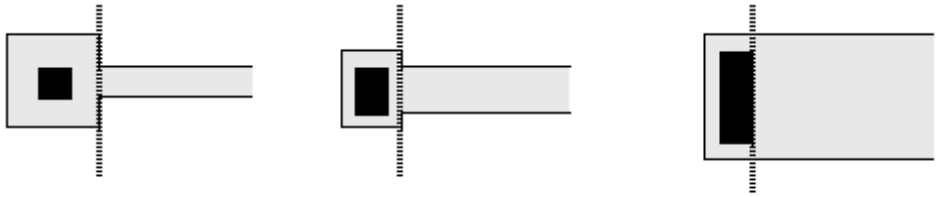
Use of dummy strips



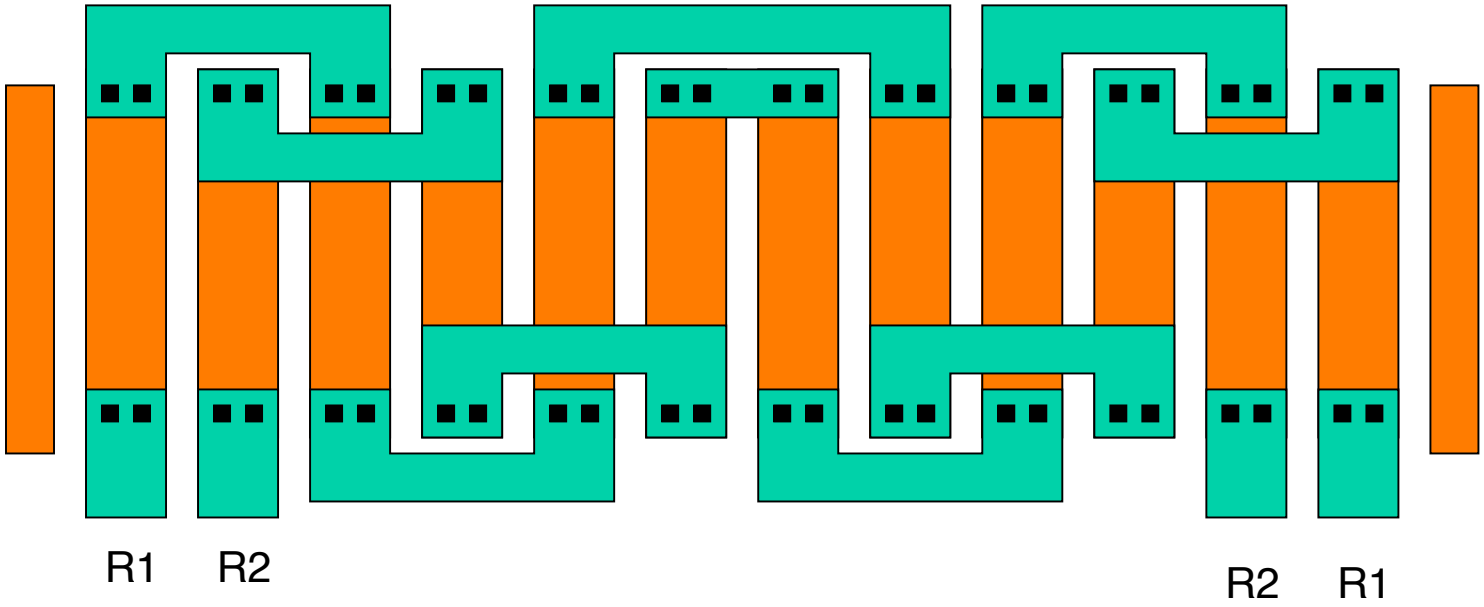
Side Diffusion



Contribution of Endings



Interdigitized and Common Centroid



121212212121

Exercise: draw a 121212121212 connection and compare the two solutions
Exercise: draw a common centroid structure (12 elements per resistor)

Resistor Guidelines

For matching :

- Use of equal structures
- Not too narrow (W = 10 mm)
- Interdigitize
- Thermal effect compensation
- 45^{o} orientation (if stressed)

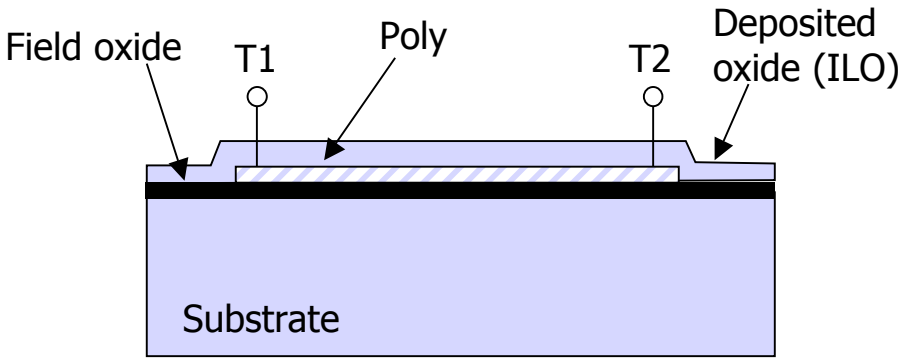
For good TC :

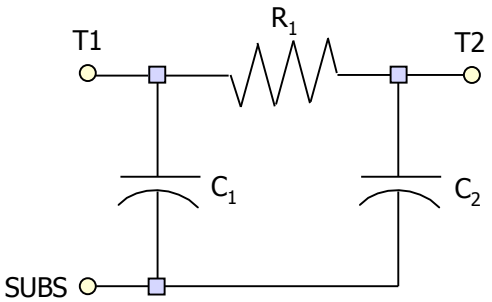
- Use of n+ or p+ layers
- Use of poly layers

For absolute value :

- Use of diffused layers
- Suitable endings

Simple Model





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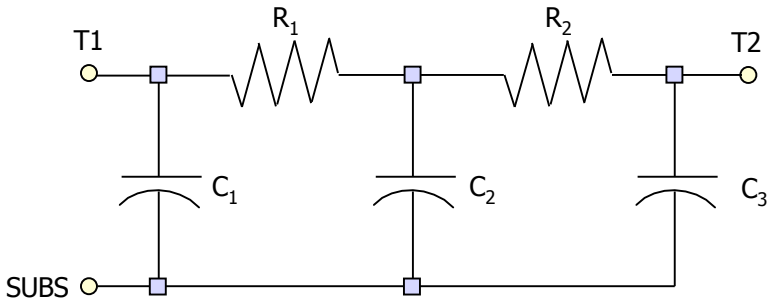
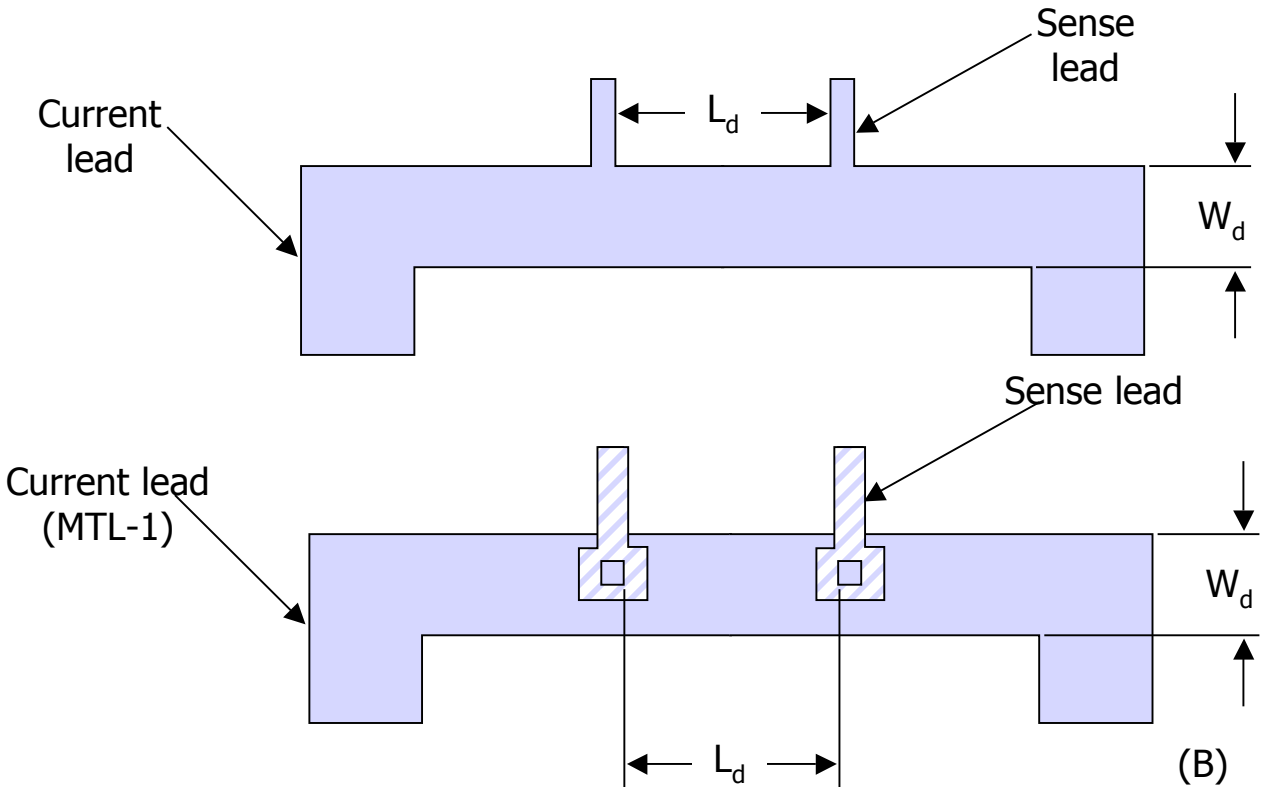


(B)

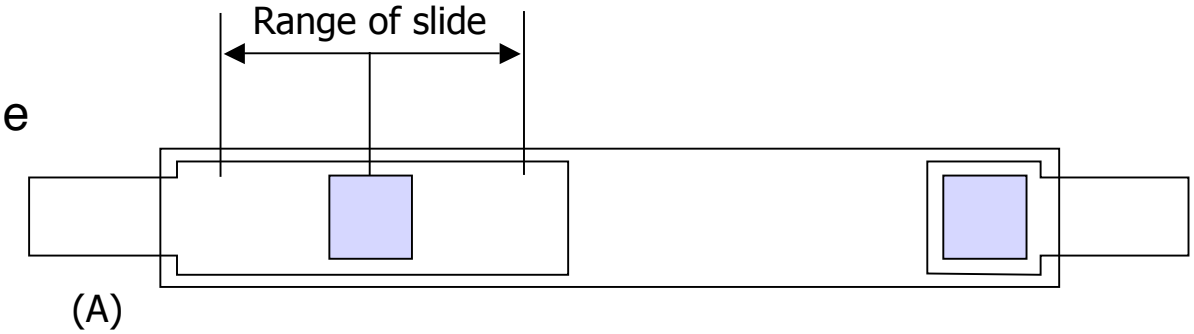
Metal Resisitors

The sheet resistance of Al metallization is around 100 mΩ/ □

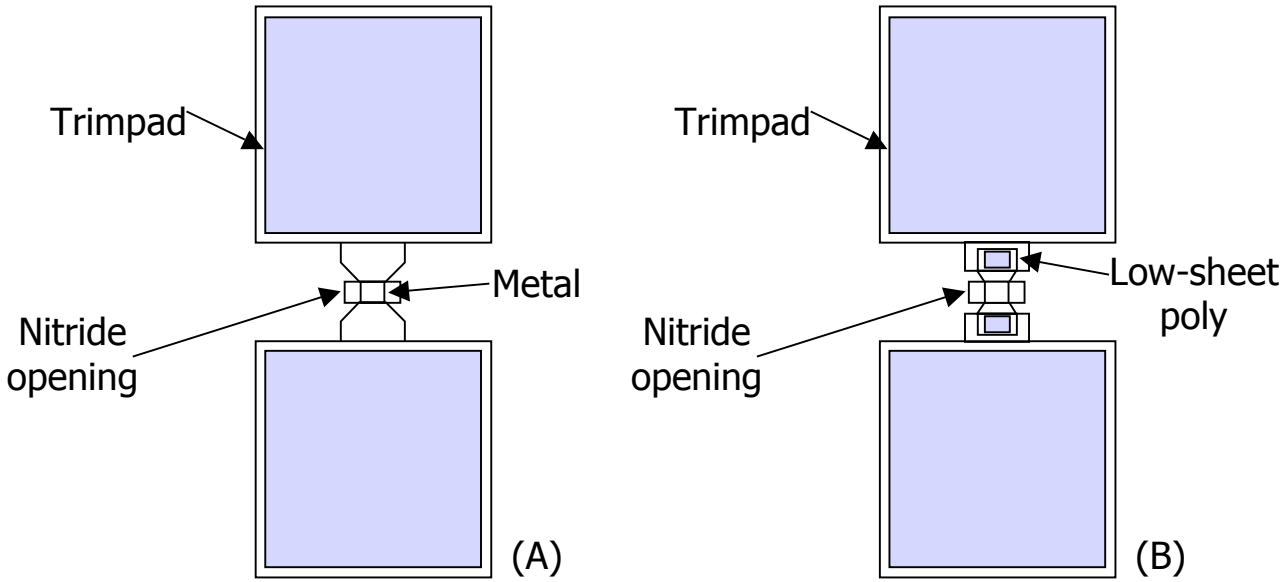


Adjusting Resistor Values

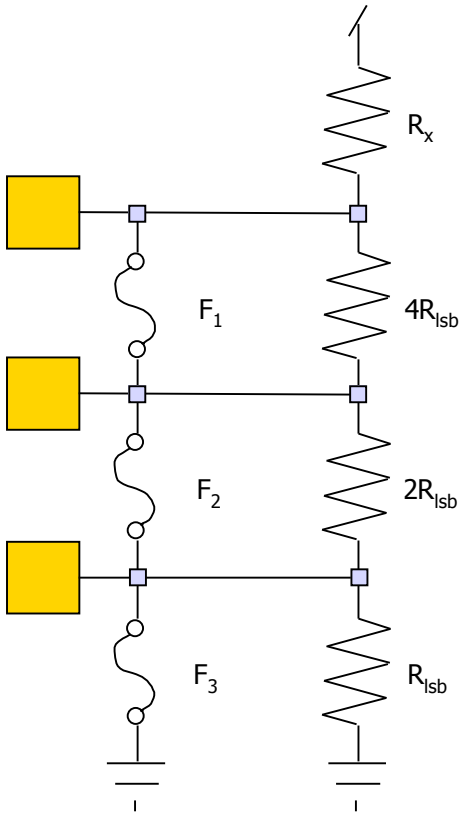
Sliding contact:
requires to change the
contact mask only



Metal fuse
and
Poly-fuse



Use of Fuses To Adjust Resistors



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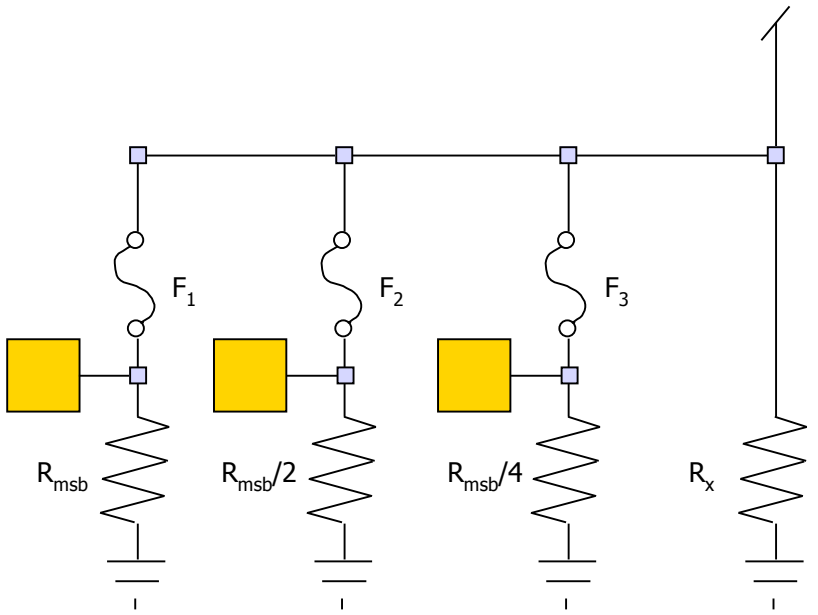

(B)

Rules for Resistor Matching

- Use the same material
- Identical geometry, same orientation
- Close proximity
- Interdigitate arrayed resistors
- Use dummy elements
- Place resistors in low stress area
- Place resistors away from power devices
- Use electrostatic shielding
- Use proper endings

Integrated Resistors

- Issue to remember
  - Integrated resistors and features
  - Resistor endings
  - Make bigger resistors integer multiples of the unit resistor
  - Finger two or more resistors for matching
  - Do not snake a resistor; use metal to make turns
  - Well under the resistor to shield from interference
  - Substrate bias around the resistor