6. CMOS Comparators

Analog Integrated Circuit Design
Franco Maloberti
Performance characteristics

A comparator detects if its input (voltage or current) is higher or lower than a reference level.

Its output is a large voltage which is assumed to represent a digital 1 or 0 level.
**Sensitivity** is the minimum input voltage that produces a consistent output. The output peak-to-peak swing is in the range of 3-5 V. Therefore, for low speed, in order to detect a 1 mV signal a voltage gain of 5000 is required.

**Input offset** is the voltage that must be applied to the input to get the transition between the low and the high state (same as the op-amp).

**Response time** is the time interval between the application of a step input and the time when the output reaches the respective logic level. The response time depends on the amplitude of the step input.
Overdrive recovery time
If the input is driven with a voltage larger than the one required to cause the output saturation, the comparator is overdriven. The response time for a given input amplitude, depends on the value of the overdrive voltage at which the comparator was driven.
**Latch Compatibility**
A latch command and an unlatch command stores and releases the output logic state. Typically the load setup time is around 2 ns.

**Power Supply Rejection**
Transfer function between the supply rails and the output of the comparator.

**Power Consumption**
Power dissipated at DC (static) and during the comparison (dynamic).

**Hysteresis**
The threshold voltage for rising input signals is different from the threshold voltage for falling input signals.
Design issues

A comparator is basically an open loop gain stage. The required DC gain is \( \approx 80 \text{ dB} \) (sometime more).

**Key points:**

- Gain obtained by using of complex schemes or by using cascade of simple schemes.
- How to cancel offset.
- Power supply rejection.
- Overdrive recovery.
- Power consumption
- All solution are strongly conditioned by the offset cancellation \( (V_{os} \approx 3 \div 10 \text{ mV}) \).
**Comparator gain:**

Due to the finite bandwidth of the circuit, the output voltage reaches $A_v \cdot V_{in}$ with a delay with respect to the time when the input is applied (response time $t_r$).

![Diagram showing the response time and gain]

The same output voltage is get, with the same response time, by the use of stages having different speed but different DC gain.
**Single stage**

\[ t << \tau = R_L C_L \]

\[ V_{out} = g_m R_L V_i (1 - e^{-t/\tau}) \approx V_i \frac{g_m}{C_L} t \]

The speed is increase by increasing \( g_m/C_L \).

Typically: \( g_m = 0.5 \text{ mA/V} \) \( C_L = 0.5 \text{ pF} \) \( g_m/C_L = 1/\text{ns} \)

Hence, the gain after a delay of 10 ns is 10.

An improvement is get by the use of a chain of identical stages. Under the same assumption:

\[ V_{out} = V_i \left( \frac{g_m}{C_L} \right)^n \frac{t^n}{n!} \]
For a given gain, it exists an optimum number of stages which gives the best response time. For example: a very small gain is reached using one only stage with a response time $t_1$ smaller than the one obtained with a chain of $n$ identical gain stages.

For a given gain an optimum $n$ results:

$$A_n = \frac{(n+1)^n}{n!}$$

$$t_n = (n+1)\frac{C_L}{g_m}$$

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<th>4</th>
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Offset cancellation

- Auto-zero technique
- Auto-zero in multistage comparators
- Differential schemes
- Compensation by auxiliary input stages

Auto-zero technique

Basic idea:
- Sample the offset during phase 1.
- Sum it to the signal during phase 2.
Two phase are required:
- Phase 1: auto-zero
- Phase 2: measure

**Time domain analysis:**

\[ V_{in}(T) = V_+(T) - V_-(T) = V_{os}(T) - (V_x(T) - V_{os}(0)) \]

If the offset changes slowly, \( V_{os}(0) \approx V_{os}(T) \)

**Frequency domain analysis**
(Laplace Transform):

\[ V_{in}(s) = V_x(s) + V_{os}(s)\left(1 - e^{-sT/2}\right) \]

\[ F_{os}(s) = 1 - e^{-sT/2} = 2je^{-sT/4} \sin\left(sT/4\right) \]

The low frequency components of the offset are cancelled.
Implementation of the auto-zero technique:

- During phase 1, the gain stage is in unity gain closed-loop configuration.
- During phase 1, $C_A$ acts as output load of the gain stage.
- During phase 2, the gain stage is in open loop configuration.
The finite gain $A_v$ of the gain stage produces a residual offset error.

$$V_{os, res} = V_{os} - V_{os} \frac{A_v}{1 + A_v} = V_{os} \frac{1}{1 + A_v}$$

The clock feed through at the opening of S1 determines an equivalent offset error ($V_{os,ck}$).

$$V_{os, res} = V_{os} \frac{1}{1 + A_v} + V_{os,ck}$$

If the complex gain stages are used, it is worth to compensate the stage only during the auto-zero phase.
Clock feedthrough and signal attenuation:

- The charge injected by the switch S1 is integrated onto $C_A$ and the input capacitance of the gain stage.
- The input signal is attenuated by the factor $\frac{C_A}{C_A + C_p}$.
- In order to reduce the attenuation and the equivalent offset $V_{os,ck} = \frac{Q_{ck}}{C_A + C_p}$, $C_A$ must be chosen large and $>> C_p$. 
Auto-zero in multistage comparators:

\[ A = A_1 A_2 \ldots A_n \]

\[ V_{os,res} = \frac{V_{os,2}}{A_1 A_2} \]

The offset of the 3rd stage (referred to the input) is also attenuated by a factor \( A_1 A_2 \), the offset of the 4th stage by a factor \( A_1 A_2 A_3 \), …
The clock feedthrough from S1 and S2 causes the rising of two equivalent offset voltages, $V_{os,1}$ and $V_{os,2}$ at the input of $A_1$ and $A_2$.

The resulting input offset is:

$$V_{os,res,ck} = \frac{Q_{inj,1}}{C_1} + \frac{1}{A_1} \frac{Q_{inj,2}}{C_2}$$

**Improved solution**

(sequential offset and clock feedthrough cancellation):

Drive S1 with $\Phi_1$ and S2, S3 with $\Phi'_1$.

The charge injected by S1 is collected on $C_2$, the equivalent offset is amplified by $A_1$. Since S2 is still on, the output voltage of $A_1$ is sampled and stored onto $C_2$.

An auto-zero of the effect of $V_{os,1}$ results.
The offset becomes:

\[ V_{os,\text{res,ck}} = \frac{1}{A_1} \frac{Q_{\text{inj,2}}}{C_2} \]

\( V_{os,\text{ck,1}} \) and \( V_{os,\text{ck,2}} \) must be such to not saturate \( A_1 \) and \( A_2 \) (gain of \( A_1 \) and \( A_2 \) low, suitable values of \( C_1 \) and \( C_2 \)).

Implementation:

Each gain stage can be implemented with a CMOS inverter: \( (A_v = 5 \div 20) \)
Differential schemes

The clock feedthrough due to the opening of S1 and S2 gives a common mode signal that is cancelled. The residual offset is due to the mismatching.

Fully differential blocks
- very low gain
- low gain with CMFB
- conventional fully differential amplifiers
Fully differential stage with very low gain

\[
A_v = \frac{g_{m1}}{g_{m3}}
\]

Advantage:
- CMFB not necessary

Disadvantage:
- The capacitance \( C_{gs} \) of the loads M3 and M4 acts as load for the output.

Advantage:
- CMFB not necessary
Fully differential stage with CMFB

Advantages:
- low capacitive load at the output
- gain $A_v = \frac{g_{m1}}{g_{ds3}}$

Disadvantage:
- two bias lines
Fully differential stage with CMFB, improved solution

- Minimum capacitive load at the nodes A and B.
- Low impedance output.
- Optionally the CMFB stage can be used as gain stage with single ended output.
Compensation by an auxiliary stage

It stores the offset at the output of the gain stage and uses it to cancel the input offset. During phase 1 the inputs of $A_1$ are short circuited. The output of $A_1$ goes to $A_1 V_{os,1}$.

\[
A_1 V_{os,1} + A_2 \left( V_{os,2} - V_o \right) = V_o
\]

\[
V_o = \frac{A_1}{1 + A_2} V_{os,1} + \frac{A_2}{1 + A_2} V_{os,2}
\]
Referred to the input of $A_1$, the equivalent offset is:

$$V_{os,res} = \frac{1}{1 + A_2} V_{os,1} + \frac{A_2}{A_1 (1 + A_2)} V_{os,2}$$

The switch at the input of $A_1$, S1 is opened while S2 is closed. The offset, caused by charge injection from S1, is attenuated by $(1 + A_2)$.

When the switch S2 is opened the injected charge is collected onto $C_S$ and an offset $V_{os,inj}$ amplified by $A_2$ appears at the output and it is equivalent to an input offset:

$$V_{in,os} = V_{os,inj} \frac{A_2}{A_1}$$
Implementation of the auxiliary stage

\[ g_{m1} \approx 10 \ g_{m6} \] in order to have \( A_1 \approx 10 \ A_2 \)

Degenerated current mirror:
- No additional supply current
- Bad PSRR
Latches

A comparator can be followed by a latch. The input can be differential or single ended; in the latter case one of the inputs can be replaced by a reference voltage.

During $\Phi_1$, M1-M3 and M2-M4 form two inverters with active load. The parasitic capacitances at nodes 1 and 2 are pre-charged at the logic levels. During $\Phi_2$ the latch is enabled and it assumes a stable state.
Latch with controlled current

When $\Phi_1$ comes along, both the output voltages try to rise. Because of the difference in input voltages one is faster and starts the regenerative action.
Latch with double regenerative loop

Fast and rugged.
Combination of gain stage and latch

When the strobe signal is down, the gain stage pre-charge the parasitic capacitances of the latch, when the strobe goes up, it starts the regenerative action of the latch.
Combination gain stage/latch with double regenerative loop and output flip-flop

When the latch signal $\Phi$ is on, the bias current is switched from the gain stage to the latch.
Key issues in comparator design

- Optimization of the **number of stages** to achieve the desired response time with a given power consumption
- **Offset cancellation** ← Autozero technique
- **Clock feedthrough, power supply and common mode rejection ratios** ← Fully differential structures
- **Overdrive recovery** ← Limit the voltage swing at critical nodes or when possible introduce a reset phase