Layout of Analog CMOS Integrated Circuit

Part 2
Transistors and Basic Cells Layout
Outline

- Introduction
- Process and Overview Topics
- Transistors and Basic Cells Layout
- Passive components: Resistors, Capacitors
- System level Mixed-signal Layout
Part II: Transistor and Basic Cell Layout

- Transistors and Matched Transistors
  - Layout of a single transistor
  - Use of multiple fingers
  - Interdigitated devices
  - Common Centroid
  - Dummy devices on ends
  - Matched interconnect (metal, vias, contacts)
  - Surrounded by guard ring

- Design for Layout
  - Stacked layout of analog cells
  - Stick diagram of analog cells
  - Example 1: two stages op-amp
  - Example 2: folded cascode
Single Transistor Layout

- A CMOS transistor is the crossing of two rectangles, polysilicon and active area.
- but, ... we need the drain and source connections and we need to bias the substrate or the well.

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Source and Drain Connections

- Ensure good connections

- Multiple contacts or one big contact?
Multiple or single contacts?

- Curvature in the metal layer can lead to micro-fractures
- Not important for large areas

Reliability problems, possible electro-migration
Multiple contacts: Exercise

- Consider the following design rules:
  - minimum contact 0.5 \( \mu \) m
  - spacing contact-contact 0.4 \( \mu \) m
  - minimum grid step 0.1 \( \mu \) m
  - spacing contact diffusion 0.6 \( \mu \) m

- Estimate the number of contacts and their spacing for
  - \( W = 50 \) \( \mu \) m
  - \( W = 52 \) \( \mu \) m
  - \( W = 60 \) \( \mu \) m
Matching single Transistors

- Regular (rectangular shape)
  - the W and L matter!!

- Parallel elements
  - silicon is unisotropic

- Possibly, the current flowing in the same direction
Asymmetry due to Fabrication

An MOS transistor is not a symmetrical device. To avoid channeling of implanted ions the wafer is tilted by about $7^\circ$.

Source and drain are not equivalent
Parasitics in Transistors

- Analog transistors often have a large W/L ratio

- Capacitance diffusion substrate

\[ C_{SB} = C_{DB} = (W + 2l_{diff})(L_D + 2l_{diff}) \]

- Resistance of the poly gate

\[ R_{gate} = L_{gate} R_{sq,poly} \]
Use of multiple fingers

\[ C'_{SB}; C'_{DB} \]

\[ C_{SB} = \frac{2}{3} C'_{SB} \]
\[ C_{DB} = \frac{2}{3} C'_{DB} \]

\[ C_{SB} = \frac{1}{2} C_{DB}; C_{DB} = C'_{DB} \]
Parasitic in Transistors: Exercise

- Calculate the parasitic capacitance diffusion-substrate for a 40 micron width transistor
  - one finger
  - 5 finger
  - 8 finger

- Use the design rules available and minimum diffusion length
Interdigitated Devices

- Two matched transistors with one node in common
  - Split them in an equal part of fingers (for example 4)
  - Interdigitate the 8 elements: AABBAABB or ABBAABBA

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Axis of Symmetries

(A) Common axis of symmetry

Axis of symmetry of device A

Axis of symmetry of device B

Common axis of symmetry (B) (C)

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## Interdigitiation Patterns

<table>
<thead>
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<th>Interdigitiation Pattern</th>
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**Note:** not all the patterns permit a stacked layout.
Interdigitated Transistors: Exercises

- Sketch the layout of two interdigitated transistors having $W_1=3W_2$ and split $W_2$ into 4 fingers. $M_1$ and $M_2$ have their source in common.

- Sketch the layout of three interdigitized transistors having the same width. Use the optimum number of fingers. The three transistors have the source in common.
Gradients in features are compensated for (at first approximation)

- metal and poly interconnections are more complex
Common Centroid Arrays

Cross coupling

Tiling (more sensitive to high-order gradients)
**Common Centroid Patterns**

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Ending elements have different boundary conditions than the inner elements -> use dummy

Dummies are shorted transistors
* Remember their parasitic contribution!
Matched interconnections

- Specific resistance of metal lines
- Specific resistance of poly
- Resistance of metal-contact
- Resistance of via

Minimize the interconnection impedance
Achieve the same impedance in differential paths
Keep short the width of fingers for high speed applications

\[ \Delta V = Z_{\text{int}} I \]
Matched Metal Connection
Waffle Transistor

Minimum capacitance drain-substrate and source-substrate

W not accurate
L not well defined

To be used in wide transistors whose aspect ratio is not relevant
Part II: Transistor and Basic Cell Layout

- **Transistors and Matched Transistors**
  - Layout of a single transistor
  - Use of multiple fingers
  - Interdigitated devices
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  - Dummy devices on ends
  - Matched interconnect (metal, vias, contacts)
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- **Design for Layout**
  - Stacked layout of analog cells
  - Stick diagram of analog cells
  - Example 1: two stages op-amp
  - Example 2: folded cascode
Stacked Layout

- Systematic use of stack or transistors (multi-finger arrangement)
- Same width of the fingers in the same stack, possibly different length
- Design procedure
  - Examine the size of transistors in the cell
  - Split transistors size in a number of layout oriented fingers
  - Identify the transistors that can be placed on the same stack
  - Possibly change the size of non-critical transistors
  - Use (almost) the same number of finger per stack
  - place stacks and interconnect
Stick Representation (one transistor)

- **EVEN**
  - Ending drain: d s d s d
  - Ending source: s d s d s
- **ODD**
  - S/D ending: s d s d d
  - D/S ending: d s d s s

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Multi-transistor Stick Diagram

Same width
M1 double

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Example 1 (2 stages OTA)

Assume to layout a two stages OTA

Width only are shown; Compensation network and bias are missing (!)
Possible stacks: 1 p-channel, 2 n-channel
change the size of M6 and M7 to 80 and 120 respectively
Width of each finger?
We want the same number of fingers per stack (k).
\[ W_{p1} = \frac{180}{k} \]
\[ W_{n1} = \frac{120}{k} \]
\[ W_{n2} = \frac{120}{k} \]
for M3 and M4 use 2 fingers

Only width matters
Stack Design and Interconnections

First attempt of interconnections (not completed)
Use of one Metal Layer

Use metal for carrying current!
Poly connections are not a problem (usually)
Stick Layout: Exercise

Draw the stick diagram of the two stages OTA in the following three cases:

• fingers of M6 and M7 all together

• M6 = 90 M7 = 60

• M1 and M2 in a common centroid arrangement
From Stick to Layout

- Input-Output
- Well and its bias
- Substrate bias
- Compensation
- Bias voltage
- Bias current

- Rectangular shape
- System oriented cell layout
  - Related cells with same height
  - Vdd and GND crossing the cell
  - In and Out properly placed
Example 2 (Folded Cascode)

Only Ws are shown

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Split of Transistors

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Stack Design

X=11; o=10

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Interconnection: Exercise

Sketch the source-drain interconnections of the folded-cascode
Basic Cell Design: check-list

- Draw a well readable transistor diagram
- Identify critical elements and nodes
  - Absolute and relative accuracy
  - Minimum parasitic capacitance
  - Minimum interference
- Mark transistors that must match
- Mark symmetry axes
- Analyze transistor sizing (W’s)
- Possibly, change transistor size for a layout oriented strategy
- Group transistors in stacks
- Define the expected height (or width) of the cell
- Sketch the stick diagram
  - Transistors of the same type in the same region
- Foresee room for substrate and well biasing
  - Substrate bias around the cell
  - Well-bias surrounding the well
- Define the connection layer for input-output (horizontal, vertical connections)
- Begin the layout now!!