Design of CMOS Analog Integrated Circuits

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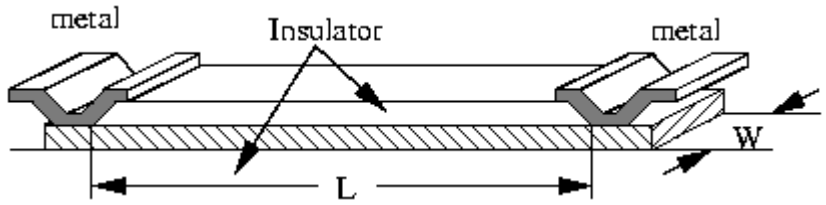
Resistors, Capacitors, Switches

TYPES OF INTEGRATED RESISTORS

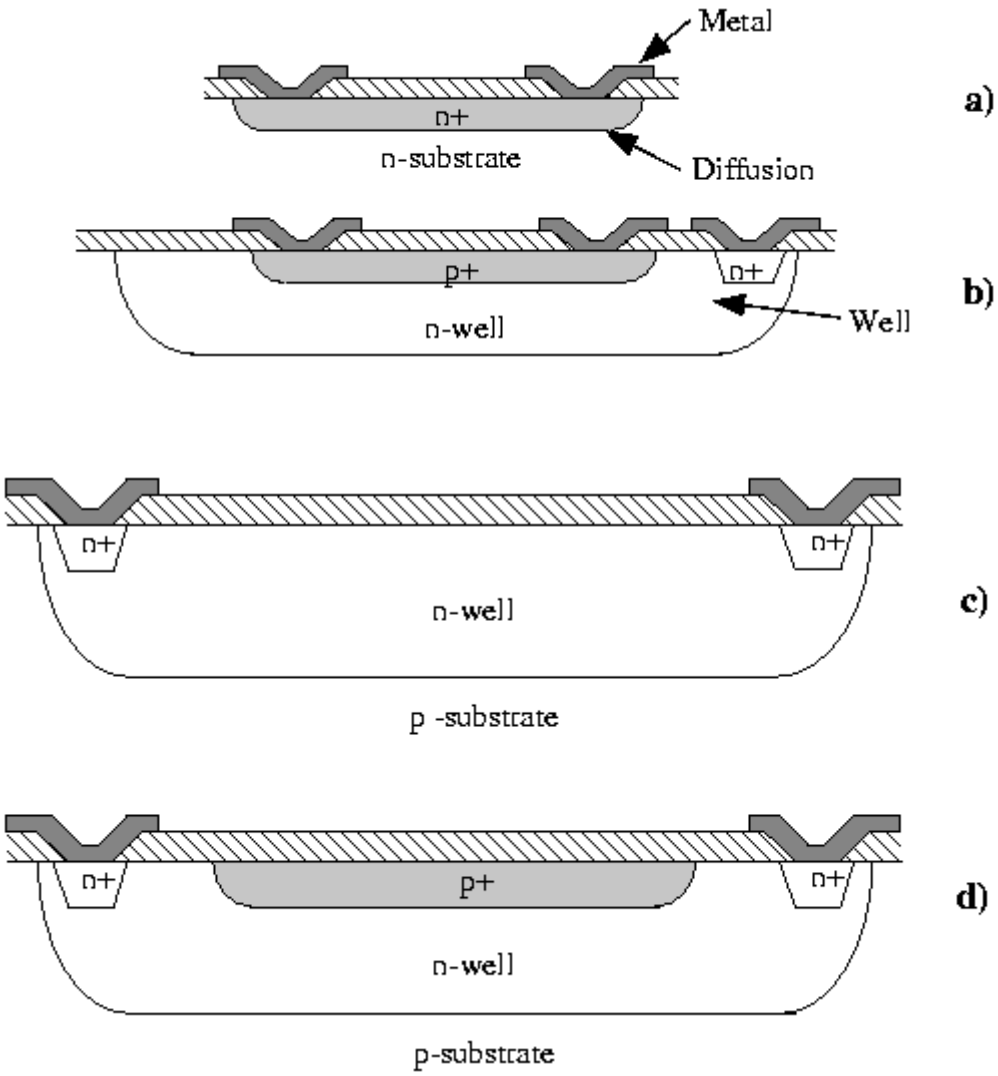
A resistor is made of a strip of resistive layer.

$$R = 2R_{cont} + \frac{L}{W} R_{\square}$$



Type of layer	Sheet Resistance Ω/□	Accuracy %	Temperature Coefficient ppm/°C	Voltage Coefficient ppm/V
n + diff	30 - 50	20 - 40	200 - 1K	50 - 300
p + diff	50 -150	20 - 40	200 - 1K	50 - 300
n - well	2K - 4K	15 - 30	5K	10K
p - well	3K - 6K	15 - 30	5K	10K
pinched n - well	6K - 10K	25 - 40	10K	20K
pinched p - well	9K - 13K	25 - 40	10K	20K
first poly	20 - 40	25 - 40	500 - 1500	20 - 200
second poly	15 - 40	25 - 40	500 - 1500	20 - 200

Types of resistances :

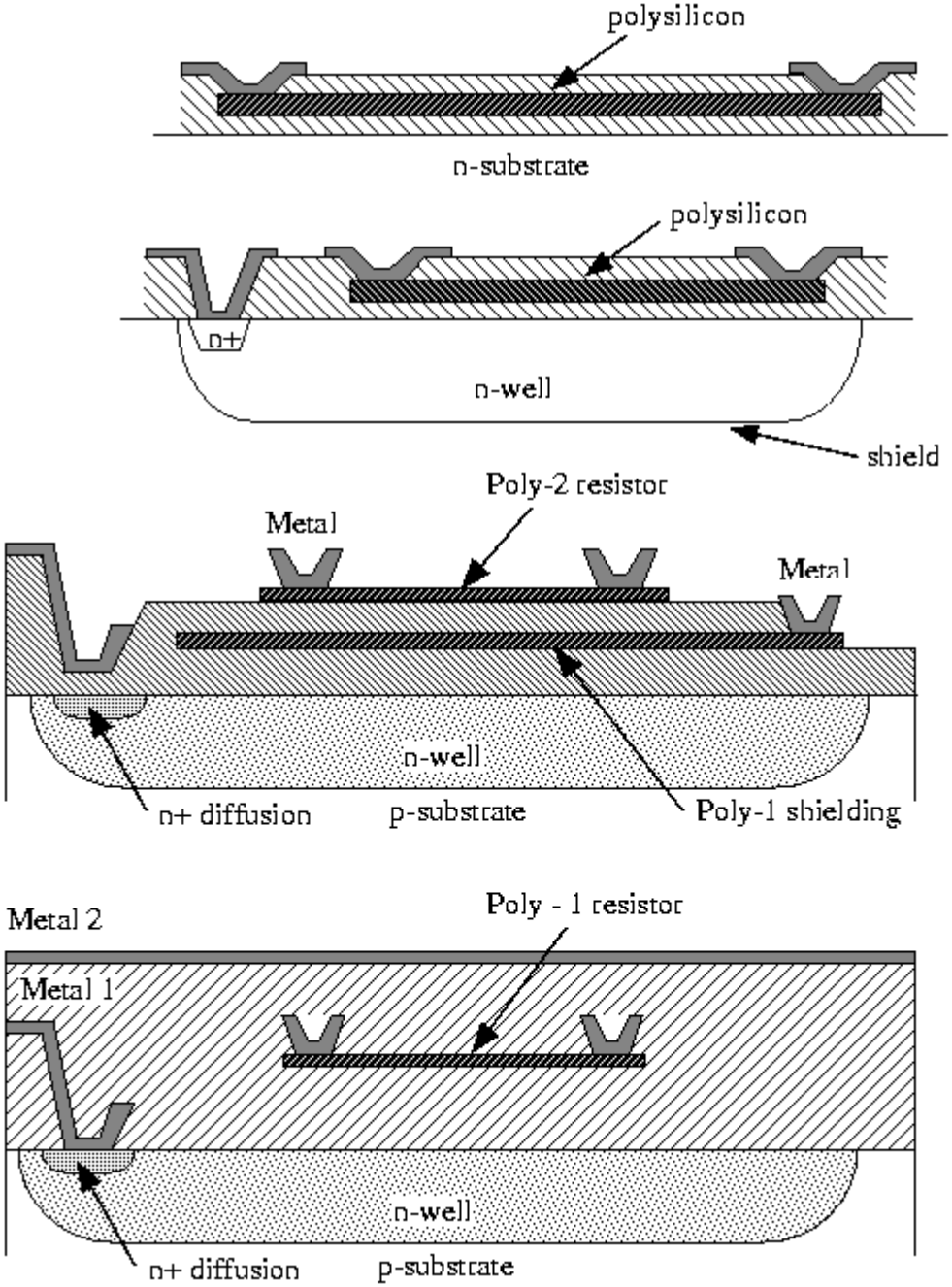


a) Diffused resistance

b) Diffused resistance intomwell

c) n-well (or p-well) resistance

d) Pinched n-well (or p-well) resistance



e) First polysilicon resistance

f) First polysilicon resistance with a well shielding

g) Second polysilicon resistance

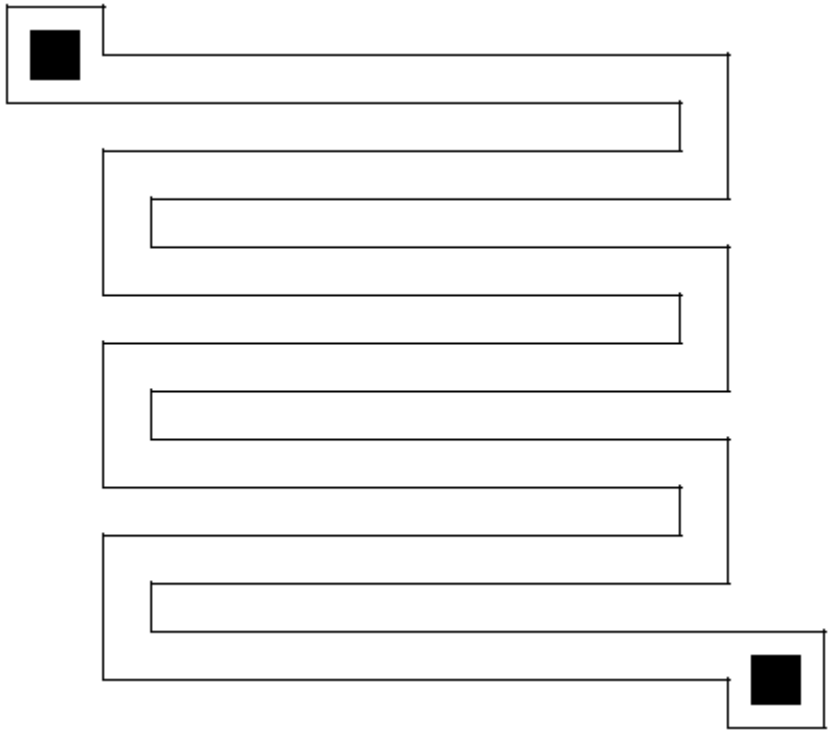
h) Second polysilicon resistance with a well shielding

In order to have large value resistors :

- Use of long strips (large L/W)
- Use of layers with high sheet resistance (bad performances)

Layout : rectangular “serpentine”

$$R = \frac{L}{W} R_{\square} = \frac{L}{W} \cdot \frac{\bar{\rho}}{x_j}$$



If the parameter are statistically independent the standard deviation of the resistance is :

$$\left(\frac{\Delta R}{R}\right)^2 = \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2 + \left(\frac{\Delta \bar{\rho}}{\bar{\rho}}\right)^2 + \left(\frac{\Delta x_j}{x_j}\right)^2$$

Since in general L >> W $\left(\frac{\Delta L}{L}\right) << \left(\frac{\Delta W}{W}\right)$

$\left(\frac{\Delta \bar{\rho}}{\bar{\rho}}\right)$ for polysilicon resistors is larger than for diffused resistors.

(Polysilicon is composed of a conglomerate of independently oriented grain of crystalline silicon)

Accuracy :

- Absolute accuracy is poor because of the large parameter drift
- Ratio (or matching) accuracy is better because it depends on the local variation of parameters.

Factor affecting accuracy :

$\left(\frac{\Delta\bar{\rho}}{\bar{\rho}}\right)$

- Polysilicon grain size
- Doping dose
- Crystal defects
- Stress
- Temperature

$\left(\frac{\Delta x_j}{x_j}\right)$

- Implant dose
- Side diffusivity
- Deposition rate

$\left(\frac{\Delta L}{L}\right);\left(\frac{\Delta W}{W}\right)$

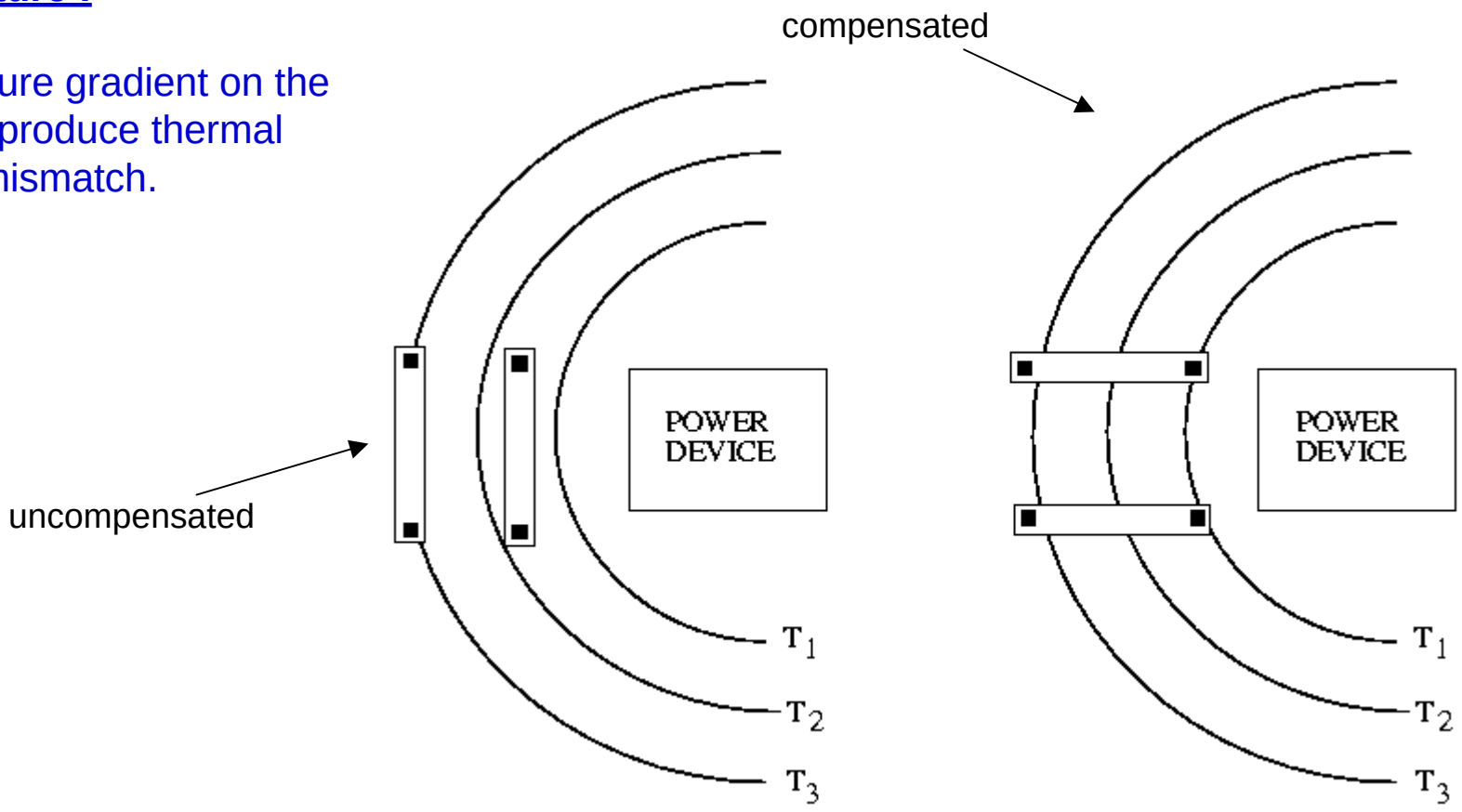
- Etching
- Boundary
- Side diffusivity

Factor affecting accuracy :

Plastic packages cause a large pressure on the die (= 800 Atm.). It determines a variation of the resistivity.
For <100> material the variation is unisotropic, so the minimum is get if the resistance have a 45^{o} orientation.

Temperature :

Temperature gradient on the chip may produce thermal induced mismatch.

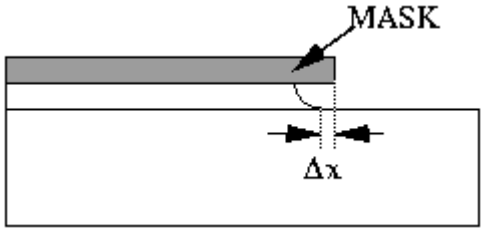


Etching :

Wet etching : isotropic (undercut effect)

H_F for SiO_2 ; H_3PO_4 for Al

Δx for polysilicon may be 0.75 - 1 μm with standard deviation 0.1 μm.



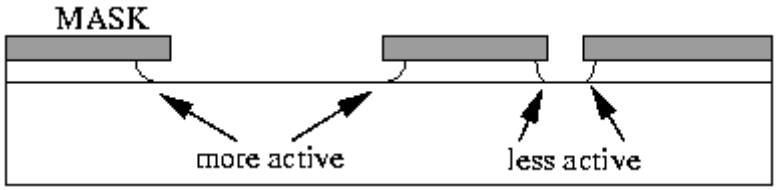
Reactive ion etching (R.I.E.)(plasma etching associated to “bombardment”) : unisotropic.

Δx for polysilicon is 0.4 μm with standard deviation 0.03 μm

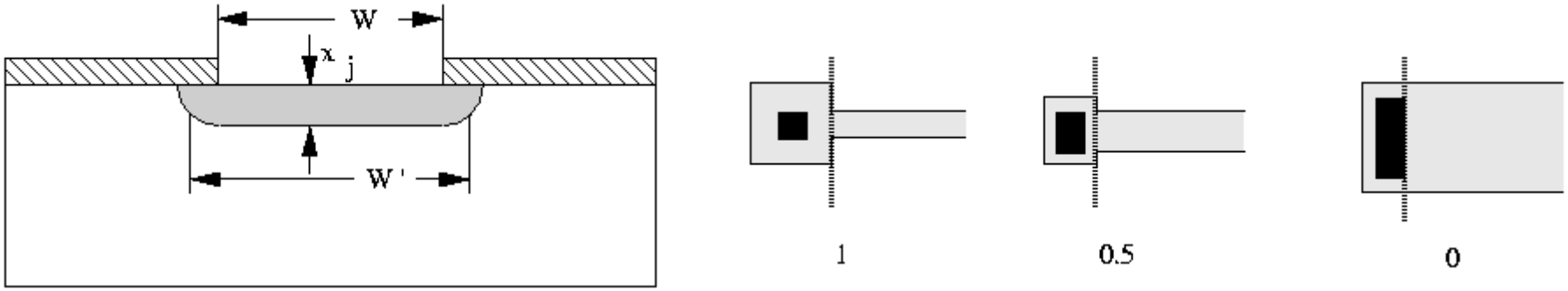
Boundary :

The etching depends on the boundary conditions

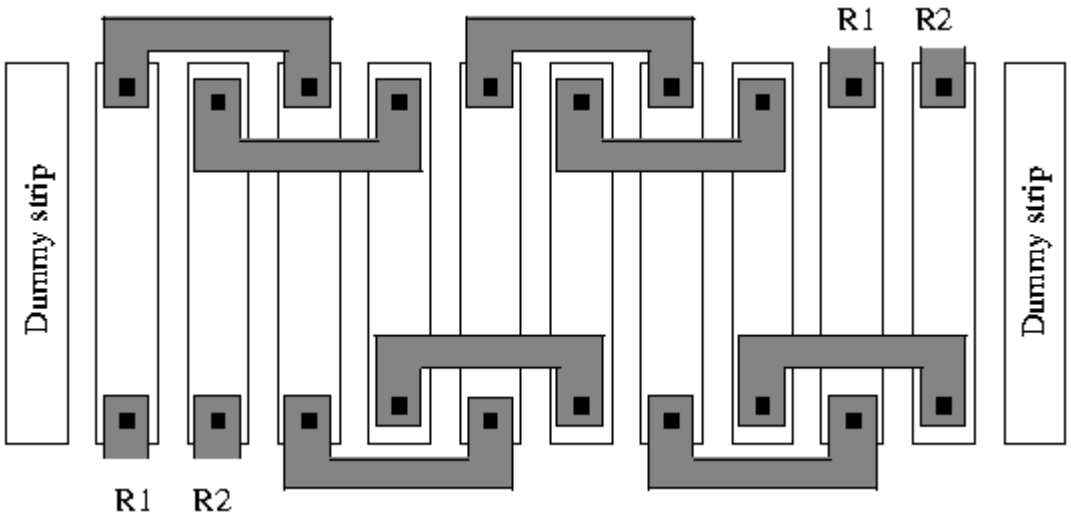
- Use of dummy strips



Side diffusion effect : Contribution of endings :



Interdigitized structure :



Resistor Guidelines

For matching :

- Use of equal structures
- Not too narrow (W = 10 μm)
- Interdigitize
- Thermal effect compensation
- 45^{o} orientation (if stressed)

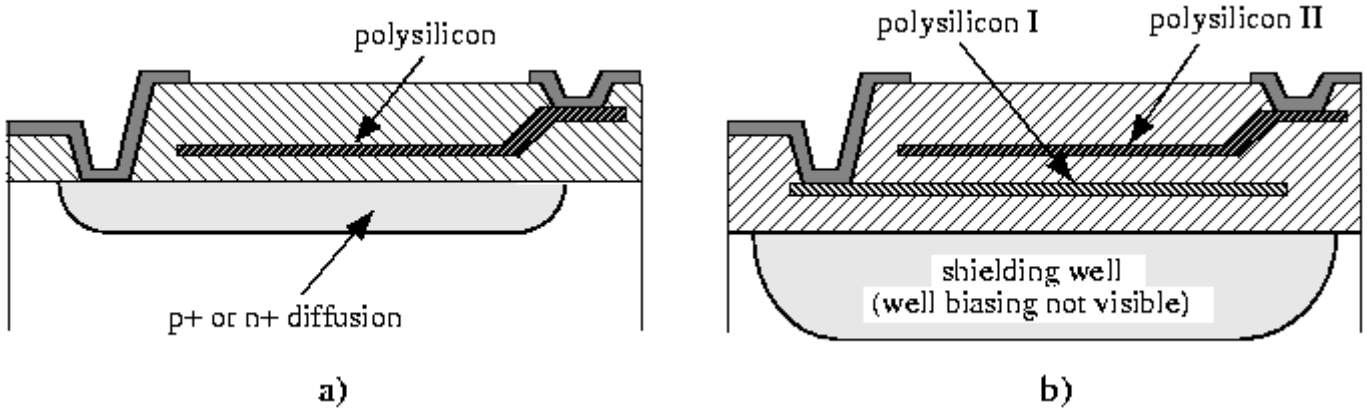
For good TC :

- Use of n+ or p+ layers
- Use of poly layers

For absolute value :

- Use of diffused layers
- Suitable endings

TYPES OF INTEGRATED CAPACITORS



Electrodes : metal; polysilicon; diffusion

Insulator : silicon oxide; polysilicon oxide; CVD oxide

$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$$

$$\left(\frac{\Delta C}{C}\right)^2 = \left(\frac{\Delta \varepsilon_r}{\varepsilon_r}\right)^2 + \left(\frac{\Delta t_{ox}}{t_{ox}}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2$$

Factor affecting accuracy :

$\left(\frac{\Delta \varepsilon_r}{\varepsilon_r}\right)$

- Oxide damage
- Impurities
- Bias condition
- Bias history (for CVD)
- Stress
- Temperature

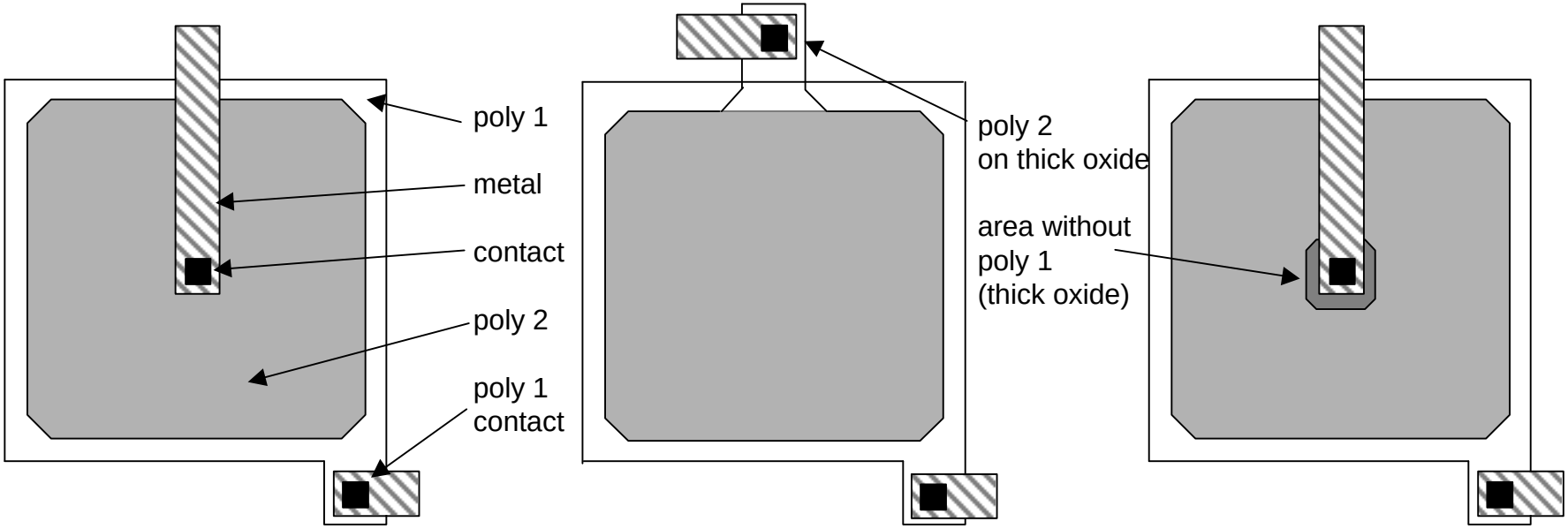
$\left(\frac{\Delta t_{ox}}{t_{ox}}\right)$

- Grow rate
- Poly grain size

$\left(\frac{\Delta L}{L}\right);\left(\frac{\Delta W}{W}\right)$

- Etching
- Alignment

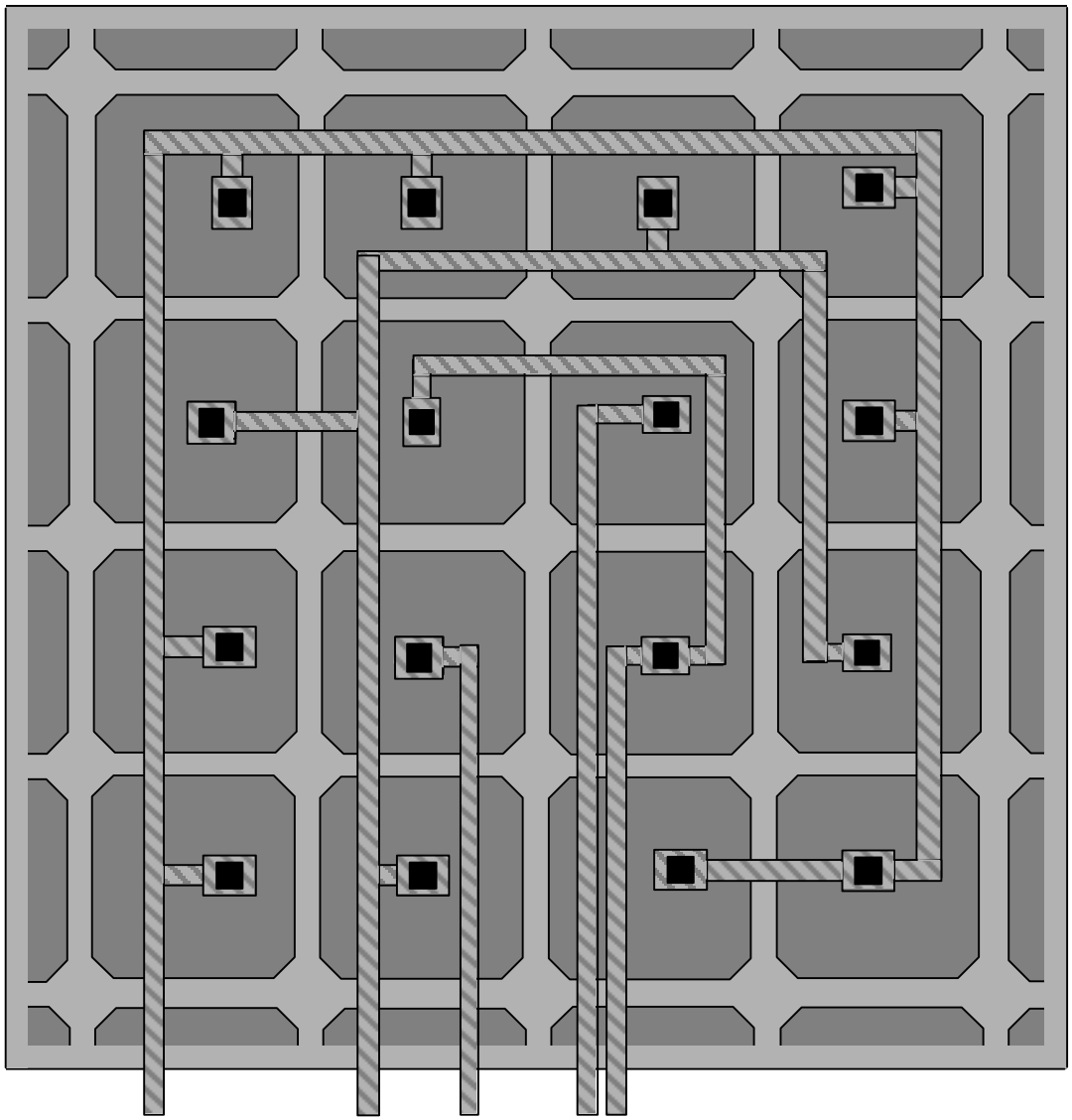
The layout of a capacitor depends on the layers used to realize the two plates :

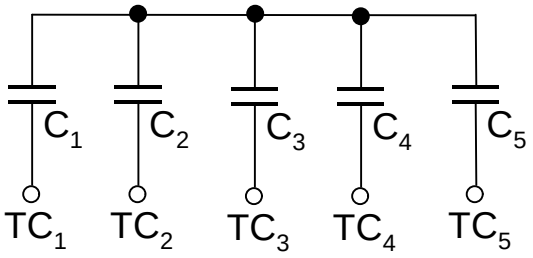


To achieve good matching :

- Use of unity capacitors connected in parallel
- Use W = L fairly large

Common centroid structures





$C_2 = C_1$
$C_3 = 2C_1$
$C_4 = 4C_1$
$C_5 = 8C_1$

Matching accuracy is better than matched resistors, because :

- $\left(\frac{\Delta\varepsilon_r}{\varepsilon_r}\right) << \left(\frac{\Delta\bar{\rho}}{\bar{\rho}}\right)$
- $\left(\frac{\Delta W}{W}\right)_{cap} < \left(\frac{\Delta W}{W}\right)_{res}$ (because the capacitors are square)
- $\left(\frac{\Delta t_{ox}}{t_{ox}}\right) < \left(\frac{\Delta x_j}{x_j}\right)$

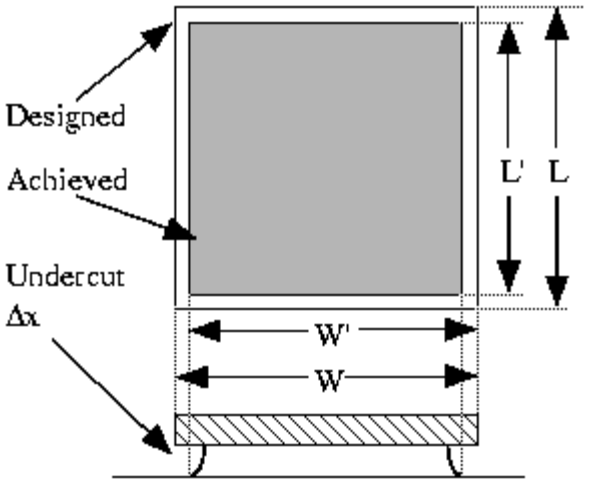
Undercut effect :

$W' = W - 2x \qquad L' = L - 2x$

Effective area :

$A' = W'L' = WL - 2(L + W)x = A - Px$

- The undercut effect gives the same proportional reduction if the perimeter-area ratio is kept constant

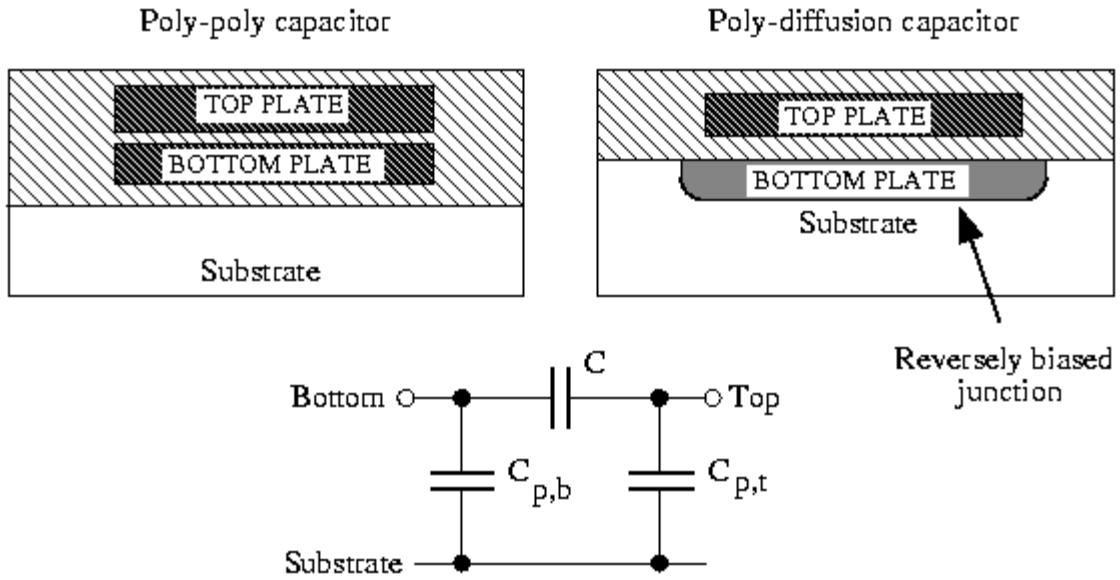


MOS capacitors features

Type	t_{ox} nm	Accuracy %	Temperature Coefficient ppm/°C	Voltage Coefficient ppm/V
poly - diff.	15 - 20	7 - 14	20 - 50	60 - 300
poly I - poly II	15 -25	6 - 12	20 - 50	40 - 200
metal - poly	500 - 700	6 - 12	50 - 100	40 - 200
metal - diff.	1200 - 1400	6 - 12	50 - 100	60 - 300
metal I - metal II	800 - 1200	6 - 12	50 - 100	40 – 200

Parasitic Capacitances :

	diffusion	poly-poly or poly-metal
$C_{p,b}$	*0.1C*	*0.01C*
$C_{p,t}$	*0.01C*	*0.001C*

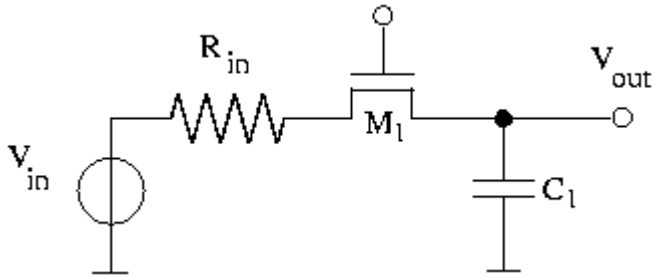


ANALOG SWITCHES

The MOS transistor is a good switch if it is used to switch charge (if used to switch current gives an offset between input and output)

In the ON-state, after a transient $V_{out} = V_{in}$, hence $V_{DS} = 0$. The MOS is in the linear region; its ON-resistance is :

$$R_{on} = \frac{1}{g_{ds}} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{Th})}$$



The value of the ON-resistance depends on the overdrive voltage, $V_{OV} = V_{GS} - V_{Th}$ and on the aspect ratio, through the transconductance parameter μC_{ox}. Modern technologies (3.3 or 2; 4 V), minimum area switch (W/L) = 1 with 1V as overdrive displays : $R_{on,n} = 8.6\ k\Omega$ $R_{on,p} = 26.3\ k\Omega$.

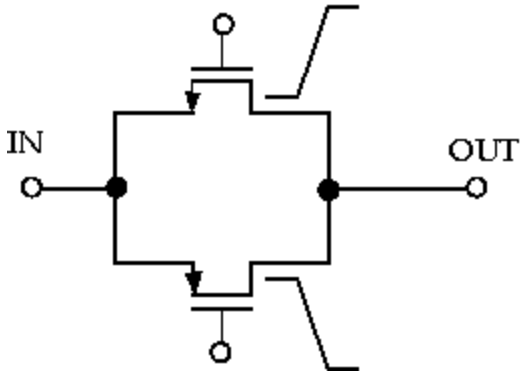
Example

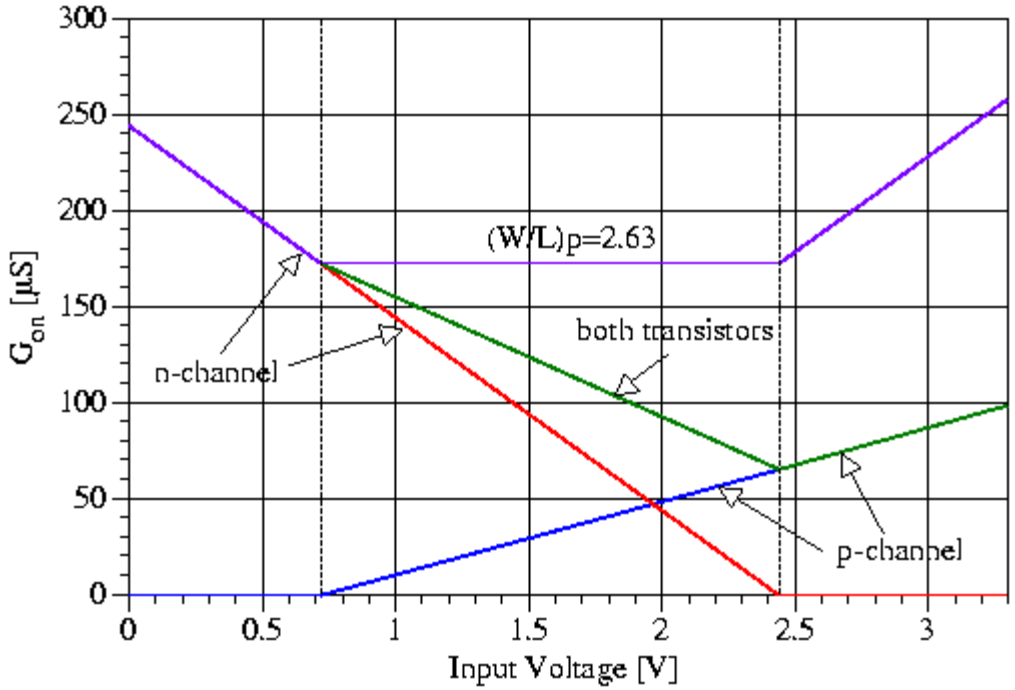
Let us assume that the switch is driven by *2 MHz* clock and remain on the on state for *250 nsec*, the capacitor is *2 pF* (rather large for integrated application). The resulting RC time constant is *17.2 nsec* and *52.6 nsec* for the n-type and p-type switch respectively. This means that we have *14.5* and *4.75* time constant available. Assuming an exponential response of the circuit (neglecting any operation in the saturation region) the output voltage reaches *0.9999995* and *0.991* of the final voltage respectively. The former result is good enough for any analog application, the latter one corresponds to an error of *0.1%* which is normally not acceptable for precise requirement. The calculation above gives the following result :

- a minimum area p-channel switch is capable of driving *2 pF* up, running at a few *MHz* clock
- a minimum area p-channel switch is capable of driving *2 pF* with a clock control not exceeding *1 MHz.*

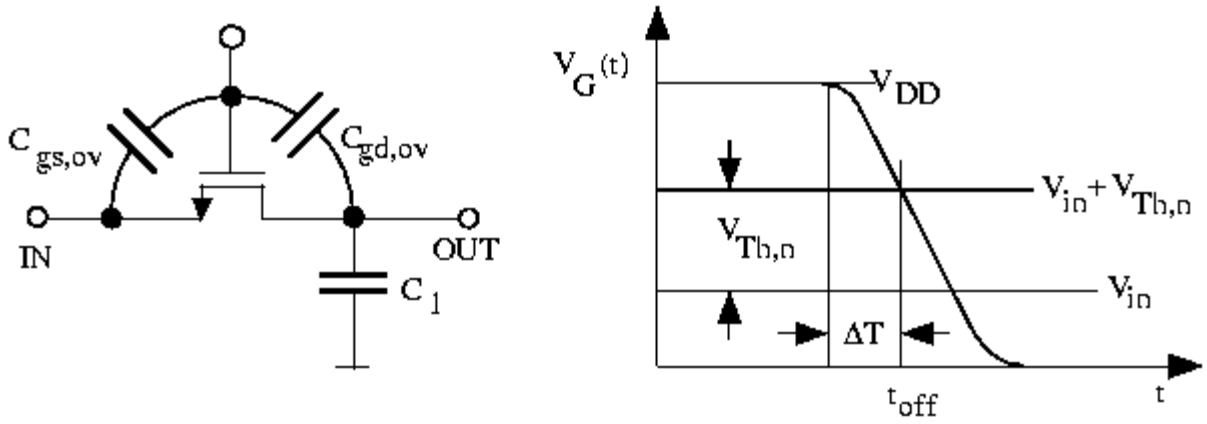
If the parallel of an n-channel and p-channel transistor is used :

The ON-conductance of the complementary switch transistor is :





CLOCK FEEDTHROUGH



In the ON-state

$$(V_G - V_{in}) > V_{Th}$$

The charge stored on the channel

$$Q_{ch} = WLC_o(V_G - V_{in} - V_{Th})$$

at the time t_{off} the charge Q_{ch} disappears.

- The charge Q_{ch} injected partially on the source and partially in the drain.
- We can assume that a fraction α of the charge from the channel affects the output node and is integrated on the store capacitor. Similarlym we analyze the charge injected from overlap capacitance.
- When the channel is still existent, the low impedance node pulls part of the charge : we assume that a fraction, β, remains in the storing capacitor.
- After t_{off}, we have no interacting injections on the two side.
- Summarizing the point above the total charge that remain in the storing capacitor :

$$C_{inj} = \alpha\{WL_{eff}C_{ox}(V_{DD} - V_{in} - V_{Th})\} + \beta\left\{\frac{Wx_{ov}C_{ox}C_1}{Wx_{ov}C_{ox} + C_1}(V_{DD} - V_{in} - V_{Th})\right\} + \frac{Wx_{ov}C_{ox}C_1}{Wx_{ov}C_{ox} + C_1}(V_{in} + V_{Th})$$

This charge, divided by the stored capacitor, gives the voltage error produced by the clock feedthrough.

CLOCK FEEDTHROUGH CANCELLATION

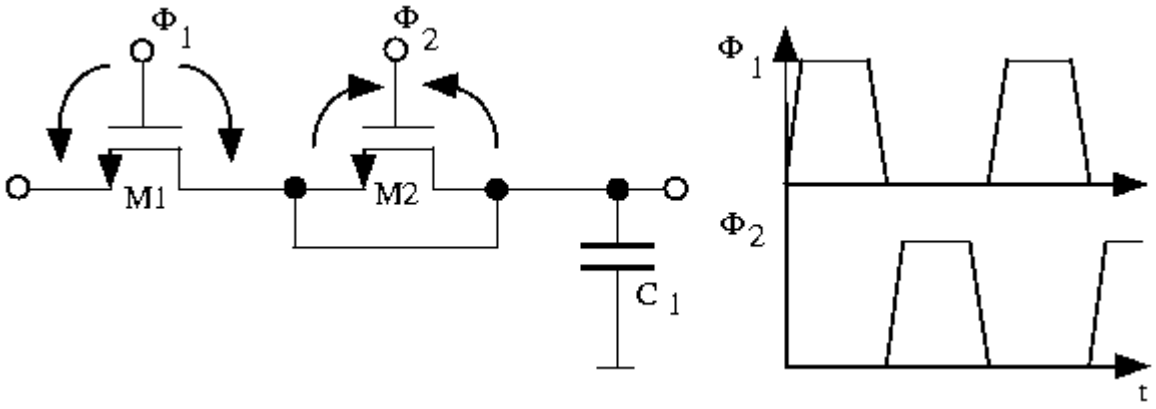
- Dummy switch
- Two complementary switch delayed driving
- Complementary switches
- Compensation scheme
- Fully differential structure

Dummy switch :

$(WL)_1 = 2(WL)_2$

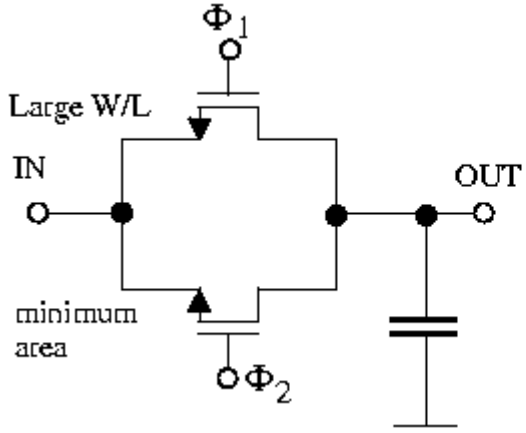
$W_1 = 2W_2$

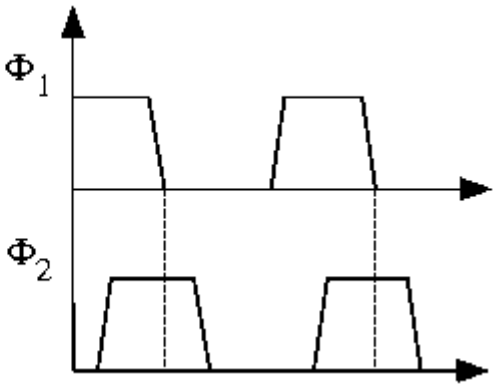
- M_2 must close after the opening of M_1

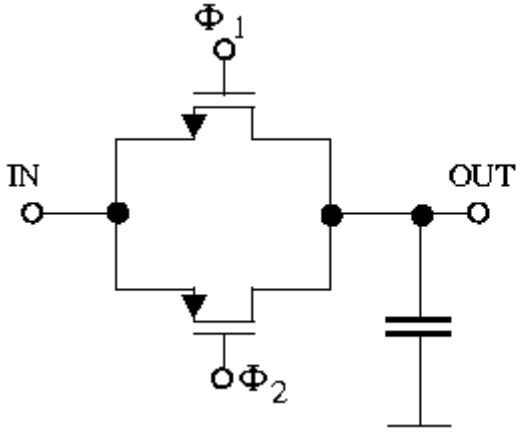


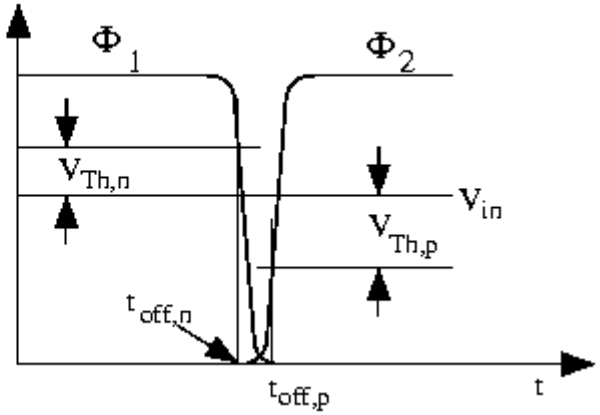
Two switches :

If a switch with non-minimum area must be used





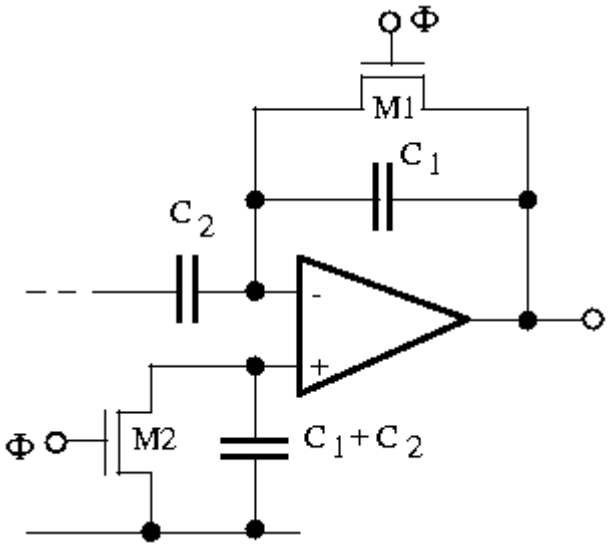


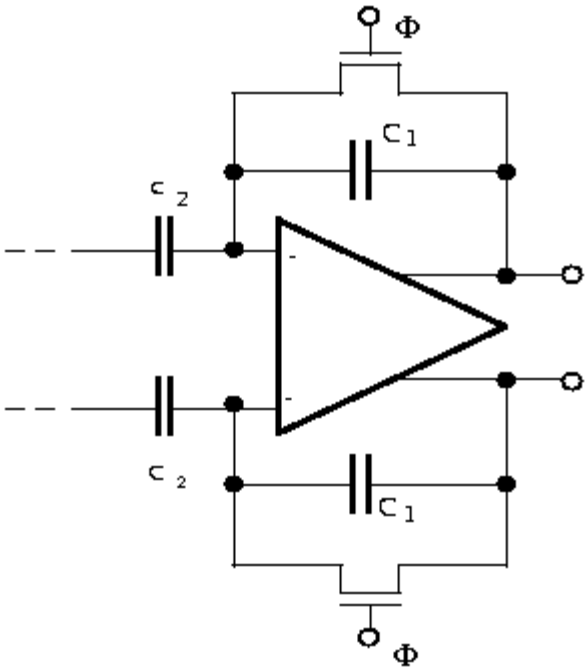


Complementary switches :

Effective only if V_{in} = constant (virtual ground)

Compensation scheme :





Fully differential structure :

The injected charge is equivalent to a common mode signal (rejected by the CMRR).