CMOS COMPARATORS
PERFORMANCE CHARACTERISTICS

- A comparator detects when its input is larger or smaller than a reference voltage. Its output is a large voltage with an appropriate sign.

- The output is assumed to represent a digital 1 or 0 level.
PERFORMANCE

**Voltage gain:** is the DC differential gain of the comparator. The output peak-to-peak swing is in the range of 3-5 V. Therefore, for low speed, in order to detect a 1 mV signal a voltage gain of 5000 is sufficient.

**Input offset:** is the voltage that must be applied to the input to get the transition between the low and the high state (same as the op-amp).

**Response time:** is the time interval between the application of a step input and the time when the output reaches the respective logic level. The response time depends on the amplitude of the step input.
**Overdrive recovery time:** if the input is driven with a voltage larger than the one required to cause the output saturation, the comparator is over driven. The response time for a given input amplitude, depends on the value of the overdrive voltage at which the comparator was driven.
**Latching compatibility.** A latch command and an unlatch command stores and releases the output logic state. Typically the load set-up time is around 2 nsec.

**Power supply rejection.** Transfer function between the supply rails and the output of the comparator.

**Power consumption.** Power dissipated at DC (static) and during the comparison (dynamic).

**Hysteresis.** The threshold voltage for rising input signals is different from the threshold voltage for falling input signals.
BASIC CONSIDERATION

- A comparator is basically an open loop gain stage. The required DC gain is ≈ 80 dB (sometime more).

**Key points:**

- Gain obtained by the use of complex schemes or by the use of the cascade of simple schemes.
- How to do $V_{os}$ cancellation.
- Power supply rejection.
- Overdrive recovery.
- Power consumption

All solution are strongly conditioned by the offset cancellation ($V_{os} \approx 3 - 10 \text{ mV}$).
Comparator Gain:

Due to the finite bandwidth of the circuit, the output voltage reaches $A_v V_{in}$ with a delay with respect to the time when the input is applied (response time $t_r$).

The same output voltage is get, with the same response time, by the use of stages having different speed but different DC gain.
Single stage:

if:

\[ t \ll \tau = R_L C_L \]

\[ V_{out} = g_m R_L V_i (1 - e^{-t/(R_L C_L)}) \approx V_i \frac{g_m}{C_L} t \]

The speed is increased by increasing \( g_m/C_L \).

typically: \[ g_m = 0.5 \text{ mA/V} \quad C_L = 0.5 \text{ pF} \quad g_m/C_L = 1/\text{nsec} \]

Hence, the gain after a delay of 10 nsec is 10.

An improvement is gained by the use of a chain of identical stages. Under the same assumption:

\[ V_{out} = V_{in} \left( \frac{g_m}{C_L} \right)^n \cdot \frac{t^n}{n!} \]
For a given gain, it exists an optimum number of stages which gives the best response time. For example: a very small gain is reached using one only stage with a response time $t_1$ smaller than the one obtained with a chain of $n$ identical gain stages.

For a given gain an optimum $n$ results:

$$A_n = \frac{(n+1)^n}{n!}$$

$$t_n = (n+1) \cdot \frac{C_L}{g_m}$$

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OFFSET CANCELLATION

- Autozero technique
- Autozero in multistage comparators
- Differential schemes
- Compensation by auxiliary input stages

AUTOZERO TECHNIQUE

Basic idea:
sample the offset during one phase and sum it to the signal during the measure phase.
Two phase are required:

Phase 1: Autozero
Phase 2: Measure

- **Time domain** analysis:
  
  \[ V_{\text{in}}(T) = V_{+}(T) - V_{-}(T) = V_{os}(T) - (V_{x}(T) - V_{os}(0)) \]

  if the offset changes slowly \( V_{os}(0) \approx V_{os}(T) \)

- **Frequency domain** analysis
  
  (Laplace Transform):

  \[ V_{\text{in}}(s) = V_{x}(s) + V_{os}(s)(1 - e^{-sT}) \]

  \[ F_{os}(s) = 1 - e^{-sT} = 2je^{-sT/2}\sin(sT/2) \]

  The low freq.of the offset are cancelled.
Autozero in single stage, implementation:

- During phase 1 the gain stage is in **unity gain closed-loop** configuration.
- During phase 1 C acts as an output load of the gain stage.
- During phase 2 the gain stage is in **open loop** configuration.
The finite gain $A_v$ of the gain stage produces a residual offset error

$$V_{os, res} = V_{os} - V_{os} \cdot \frac{A_v}{1 + A_v} = V_{os} \cdot \frac{1}{1 + A_v}$$

Exists the problem of the clock feedthrough at the opening of $S_1$; it determines an equivalent offset error ($V_{os, ck}$).

$$V_{os, res} = V_{os} \cdot \frac{1}{1 + A_v} + V_{os, ck}$$

If the complex gain stages are used it is worth to compensate the stage only during the autozero phase.
Clock feedthrough and signal attenuation:

- The charge injected by the switch $S_1$ is integrated onto $C$ and the input capacitance of the gain stage.
- The input signal is attenuated by the factor $C/(C + C_{in})$.
- In order to reduce the attenuation and the equivalent offset [$V_{os,ck} = Q_{ck}/(C + C_{in})$] $C$ must be chosen large and $>> C_{in}$.
Autozero in multistage comparators:

\[ A = A_1 A_2 \ldots A_n \]

- The offset of the third stage is referred to the input attenuated by the factor \( A_1 A_2 \). Usually its contribution is negligible.
- The clock feedthrough from \( S_1 \) and \( S_2 \) causes the rising of two equivalent offset voltages, \( V_{os,1} \) and \( V_{os,2} \) at the input of \( A_1 \) and \( A_2 \).

The resulting input offset is:

\[ V_{os} = V_{os,1} + \frac{1}{A_1} V_{os,2} \]
**Improved solution** (sequential offset and feedthrough cancellation):

Drive $S_1$ with $\Phi_1$ and $S_2$, $S_3$ with $\Phi'_1$.

- The charge injected by $S_1$ is collected on $C_2$, the equivalent offset is amplified by $A_1$. Since $S_2$ is still on, the output voltage of $A_1$ is sampled and stored onto $C_2$.

- An autozero of the effect of $V_{os,1}$ results.

The offset becomes:

$$V_{os} = \frac{1}{A_1}V_{os,2}$$

- $V_{os,1}$ and $V_{os,2}$ must be such to not saturate $A_1$ and $A_2$ (gain of $A_1$ and $A_2$ low, suitable values of $C_1$ and $C_2$).
Implementation:

- Each gain stage can be implemented with a CMOS Inverter: \( (A_v = 5 - 20) \)

Differential schemes:

- The clock feedthrough due to the opening of S1 and S2 gives a common mode signal. Its effect is cancelled. Residual offset is due to the mismatching.
**Fully differential blocks:**

- Very low gain
- Low gain with CMFB
- Conventional fully differential amplifier

**Very low gain:**

- **Advantage:** CMFB not necessary
- **Disadvantage:** The capacitance $C_{gs}$ of the loads $M_3$ and $M_4$ act as load of the output.
**Low gain with CMFB:**

- Low capacitive load at the output
- \[ \approx \frac{1}{2} C_{gs, A} + \ldots \]
- Two bias lines

**Improved solution:**

- Minimum capacitive load at the nodes A and B.
- Low impedance output.
- Optionally the CMFB stage can be used as gain stage with single ended output.
Compensation by auxiliary input stages:

**Basic idea:** store the offset at the output of the gain stage and use it in feedback connection to cancel the input offset.

During phase 1 the inputs of $A_1$ are short circuited. The output of $A_1$ goes to $A_1V_{os,1}$

$$A_1V_{os,1} + A_2(V_{os,2} - V_o) = V_o$$

$$V_o = \frac{A_1}{1 + A_2} V_{os,1} + \frac{A_2}{1 + A_2} V_{os,2}$$
Referred to the input of A1, the equivalent offset is:

\[ V_{eq, \text{os}} = \frac{V_{os, 1}}{1 + A_2} + \frac{V_{os, 2}}{A_1} \]

- The switch at the input of A1, S1 is opened while S2 is closed. The offset, caused by charge injection from S1, is attenuated by \((1 + A_2)\).

- When the switch S2 is opened the charge that it inject is collected onto \(C_{AZ}\) and an offset \(V_{os, \text{inj}}\) appears. It is amplified by \(A_2\) and appears at the output; it is equivalent to an input offset equal to:

\[ V_{in, \text{os}} = V_{os, \text{inj}} \left( \frac{A_2}{A_1} \right) \]
\( g_{m1} \approx g_{m6} \) in order to have \( A_1 \approx 10 \, A_2 \)

**Degenerated current mirror:**

- No additional supply current
- Bad PSRR
A comparator can be followed by a latch. The input can be differential or single ended; in the latter case one of the inputs can be replaced by a reference voltage.

During $\Phi_1$ $M_1$, $M_3$ and $M_2$, $M_4$ form two inverters with active load. The parasitic capacitances incident nodes 1 and 2 are pre-charged to a logic signals.
During $\Phi_2$ the latch is enabled and it assumes a stable state.

Typically: latching time 2-10 nsec with $V_{in} = 10$ mV

When $\Phi_1$ comes along, the output voltages will both try to rise. Because of the difference in input voltages one is faster and starts the regenerative action.
Strobed at the drain: carrier mobility faster at zero substrate bias.

Small load capacitance of the flip-flop.
Combination gain stage / latch:

- When the strobe signal is down, the gain stage pre-charge the parasitic capacitances of the latch, when the strobe goes up, starts the regenerative action of the latch.
Combination gain stage / latch with double regenerative loop and output flip-flop:

- When the latch signal $\Phi$ is on, the bias current is switched from the gain stage to the latch.
POWER CONSUMPTION

Comparator gain including offset compensation and output latch

The voltage swing at the output of the first stage is

\[ V_o(t) = \frac{g_{m,1}}{C_1} \int_0^t V_i(t) \, dt \]

The voltage swing at the output of the second stage is:

\[ V_{out}(t) = \frac{g_{m,2}}{C_2} \int_0^t V_o(t) \, dt \]
For constant or slowly varying signal at the end of the comparison phase ($\gamma / f_{ck}$) the output voltage $V_{out}$ is

$$V_{out} = \frac{1}{2} V_i \frac{g_{m,1} g_{m,2}}{C_1 C_2} (\gamma / f_{ck})^2$$

Theoretical minimum of power consumption

MOS transistors in strong inversion ($I_D > I_{lim}$)

$$g_m = \sqrt{\frac{2 \mu C_{ox} I_D W}{n L}}$$

MOS transistors in weak inversion ($I_D < I_{lim}$)

$$g_m = \frac{q I_D}{n k T}$$
The limit between strong and weak inversion is

\[ I_{\text{lim}} = 2\eta \mu C_{oc} \frac{W}{L} \left( \frac{kT}{q} \right)^2 \]

If the input voltage of a gain stage exceeds the critical value \( V_{\text{crit}} = n kT/q \) or \((V_{GS} - V_{\text{th}})/2\) the output current saturates to the maximum value \( I_D \)

To achieve a given \( V_{\text{out}} \) the current in the second stage must be

\[ I_{D,2} > \frac{V_{\text{out}} C_2 f_\text{ck}}{\gamma} \]

The current in the first stage can be obtained from

\[ g_{m,1} > \frac{V_{\text{crit}} C_1 f_\text{ck}}{V_{i,\text{min}} \gamma} \text{ for } V_{i,\text{min}} < V_{\text{crit}} \text{ or} \]
Theoretical minimum of power consumption

In practical cases security margins have to be taken into account

\[ I_{D,1} > \frac{V_{\text{crit}} C_1 f_{\text{ck}}}{\gamma} \text{ for } V_{i,\text{min}} > V_{\text{crit}} \]
CONCLUSIONS

- **Key issues** in comparator design
  - Optimization of the *number of stages* to achieve the desired *response time* with a given *power consumption*
  - Offset cancellation → **Autozero** technique
  - *Clock feedthrough, power supply* and *common mode* rejection ratios → Fully differential structures
  - **Overdrive recovery** → Limit the voltage swing at critical nodes or when possible introduce a *reset* phase