DESIGN OF CMOS ANALOG INTEGRATED CIRCUITS

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Continuous Time and Switched Capacitor Filters
OUTLINE

☐ Electrical Filters
☐ Single op-amp realization
☐ Cascade and multiple loop feedback
☐ Switched capacitor technique
☐ Biquadratic SC filters
☐ SC N-path filters
☐ Finite gain and bandwidth effects
☐ Layout consideration
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ELECTRICAL FILTERS

- Electrical filters is an interconnection network of electrical components which operates a modification of the frequency spectrum of an applied electrical signal.
- The network is linear and time invariant.

FILTER DESIGN PROCEDURE:

- Filter specifications
- Design of the network that implements the specifications
- Component values evaluation
**Filter specification:**

Is usually defined by a mask which specifies the range of allowed frequency responses.

The frequency range is divided into:

- Pass band
- Stop band
Usually, they are specified:

- Ripple in the pass band
- Attenuation in the stop band

Specification of the phase response:

- Usually linear phase response

\[ \Phi(f) = k(f - f_0) \]

Type of filters:

- Low pass, low pass notch
- High pass, high pass notch
- Band pass, band reject
- All pass
 Networks:

Filter specifications are met with linear networks which determine a transfer function of the form:

\[ H(s) = \frac{P_m(s)}{Q_n(s)} \]

\(P_m(s)\) and \(Q_n(s)\) are polynomial of order \(m\) and \(n\) respectively. The zeros of \(P_m(s)\) are the zeros of the transfer function. The zeros of \(Q_n(s)\) are the poles of the transfer function. Always \(n \geq m\).

The number of poles gives the order of the filter.

- The ripple in the pass-band and the transition between the stop-band and the pass-band determine the order of the filter.
• Transmission zeros in the stop-band help in getting a sharper transition

• Very elementary specifications are met with first order or second order filters.

**First order:**

\[ H_{LP} = \frac{1}{1 + sRC} \]

\[ H_{HP} = \frac{sRC}{1 + sRC} \]

**Second order filter or biquadratic (biquad) filter:**
\[ H(s) = k \cdot \frac{s^2 + \frac{\omega_z}{Q_z} + \omega_z^2}{s^2 + \frac{\omega_0}{Q_0} + \omega_0^2} = \frac{p_0 + sp_1 + s^2p_2}{s^2 + \frac{\omega_0}{Q_0} + \omega_0^2} \]

Low pass response:

\( \omega_z \rightarrow \infty \quad k \rightarrow (p_0/\omega_z^2) \quad p_0 = 1 \quad p_1 = 0 \quad p_2 = 0 \)

High pass response:

\( p_0 = 1 \quad p_1 = 0 \quad p_2 = 0 \quad \omega_z = 0 \)

Low pass notch response:

\( p_0 = 0 \quad \omega_2 > \omega_1 \)

High pass notch response:
\[ p_1 = 0 \quad \omega_2 < \omega_p \]

Band pass response:

\[ p_0 = 0 \quad p_1 = k \frac{\omega_z}{Q_z} \quad p_2 = 0 \]

All pass response:

\[ p_0 = \omega_0^2 \quad p_1 = -\frac{\omega_0}{Q_0} \quad p_2 = 1 \]
Active realization of biquadratic transfer functions:

\[-sC_1 V_1 = Y_1 V_{in} + Y_3 V_0\]

\[(sC_2 + G_2) V_0 = Y_2 V_{in} + G_3 V_1\]

Eliminating $V_1$ it results:
\[ \frac{V_0}{V_{in}} = \frac{sC_1 Y_2 - G_1 Y_1}{sC_1(sC_2 + G_2) + G_1 Y_3} \]

- Note that, for stability reasons, the inverter and a dumping (\(R_2\) or dissipative \(Z_3\)) are requested around the loop
- The admittances \(Y_1\), \(Y_2\) and \(Y_3\) have usually the form \(Y = G + sC\)

\[
-sC_1 V_1 = Y_1 V_{in} + Y_3 V_0 \\
-(sC_2 + G_2)V_0 = Y_2 V_{in} + G_1 V_1 \\
\frac{V_0}{V_{in}} = \frac{sC_1 Y_2 - G_1 Y_1}{sC_1(sC_2 + G_2) + G_1 Y_3}
\]
SINGLE OP-AMP REALIZATION

- Sallen and Key filter:

\[ H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{Z'_1 Z'_2}{(Z_1 + Z_2 + Z'_2) Z'_1 + Z_1 Z_2} \]
For low pass response:

\[ Z_1 = Z_2 = R \quad Z'_1 = \frac{1}{sC_1} \]

\[ Z'_2 = \frac{1}{sC_2} \]

\[ H(s) = \frac{1}{1 + 2sRC_2 + s^2R^2C_1C_2} \]

For maximally flat response: \( Z_1 = \sqrt{2}/2 ; \quad C_1 = 2C_2 ; \quad f_p = \frac{1}{2\pi RC_\sqrt{2}} \)

Key features:

- The op-amp is in buffer connection, input swing must be equal to the output swing.
- In the pass-band no current flows on the resistances (even if they are non linear, non harmonic distortion results).
Rauch filter

\[ H(s) = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{1}{Z_1 + \frac{Z_2}{Z_3} + \frac{Z'_2}{Z'_1 + \frac{Z_1}{Z_2 + \frac{Z_1}{Z_3}}}} \]
For low pass response:

\[ Z_1 = R_1 \quad Z_2 = R_2 \quad Z_3 = R_3 \]

\[ Z'_1 = \frac{1}{sC_1} \quad Z'_2 = \frac{1}{sC_2} \]

\[ H(s) = -\frac{1}{R_1} + sC_2 \left( \frac{R_1}{R_3} + \frac{R_1 R_2}{R_3} \right) + s^2 R_1 R_2 C_1 C_2 \]

For maximally flat response:

\[ R_1 = R_3 = 2R_2 = 2R; \quad C_1 = 4C_2 = 4C \]

\[ f_p = \frac{1}{4\pi RC \sqrt{2}} \]
Key features:

- The op-amp has the non inverting input referred to the ground.
- In the pass-band there is a current flowing into the resistors.

**Low pass Sallen and Key filter with real op-amp:**

A real op-amp used in CMOS monolithic S&K filter is a transconductance op-amp
With the above equivalent scheme:

\[
H(s) = \frac{1 + 2sC/g_m + 2s^2RC^2/g_m}{\alpha + s\beta + s^2\gamma + s^3\delta}
\]

\[
\alpha = 1 + \frac{1}{A_0} \quad \beta = 2RC + \frac{R_0C_0 + 2R_0C + 4RC}{A_0}
\]

\[
\gamma = 2R^2C^2 + \frac{1}{A_0}(4RR_0C(C + C_0) + 2R^2C^2) \quad \delta = 2 \cdot \frac{R^2C^2}{C_0}g_m \quad A_0 = g_mR_0
\]

The transfer function has two zeros and three poles.
If \( k = Rg_m >> 1 \) the zeros are practically complex conjugates and are located at

\[
\omega_0 = \sqrt{g_m/2RC^2} = \omega_p\sqrt{k}
\]

The extra-pole is real and is located around the GBW of the op-amp.
A low value of $k = Rg_m$ determines a shift of the poles of the S & K filter with respect to the designed position.
**Design criteria:**

- Use an op-amp with $f_T > 20 \ f_p$
- Use resistances $R > 40/g_m$
Low pass Rauch filter with real op-amp:

\[ H(s) = \frac{-1 + s(R + R_0)C/(A_0 + 1)}{\alpha + s\beta + s^2\gamma + s^3\delta} \]

\[ \alpha = 1 + \frac{4}{A_0 - 1} \]

\[ \beta = 4RC + \frac{2R_0C_0 + R_0C + 13RC}{A_0 - 1} \]

\[ \gamma = 8R^2C^2 + \frac{6RR_0CC_0 + 2RR_0C^2 + 18R^2C^2}{A_0 - 1} \]

\[ \delta = 8 \cdot \frac{R^2R_0C_0C^2}{A_0 - 1} g_m \]

- The transfer function has one zero and three poles.
- The zero is far away from \( f_p \) if \( A_0 \gg 1 \)
The extra-pole is around the unity gain frequency of the op-amp.

The two other poles are shifted with respect to the designed location.
**Effect of the integrated resistors:**

\[ Y = \frac{\sqrt{sC/R}}{\sinh \sqrt{sRC}} \]

\[ Y_P = Y(\cosh(\sqrt{sRC} - 1)) \]

![Diagram of integrated resistor effect](image)

![Graphs showing gain vs. log(f)](image)
HIGH ORDER FILTERS

There are several ways to realize high order (> 2) filters. We will consider:

- Cascade realization
- Multiple loop feedback

**Cascade realization:**

Consists in the cascade connection of isolated biquad sections. $H_i(s)$ is the biquad transfer function.
For getting isolation it must be:

\[ R_s \ll Z_{in, 1} \quad Z_{out, i} \ll Z_{in, i + 1} \quad Z_{out, N} \ll R_L \]

\[ H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \prod_{i=1}^{N} H_i(s) \]

A given specification is met with a rational transfer function:

\[ F(s) = \frac{a_0 + a_1 s + a_2 s^2 + \ldots + a_m s^m}{b_0 + b_1 s + b_2 s^2 + \ldots + b_n s^n} = \frac{a_m}{b_n} \cdot \prod_{i=1}^{m} \frac{(s - s_{zi})}{\prod_{i=1}^{m} (s - s_{pi})} \]

\( s_{zi} \) and \( s_{pi} \) are the zeros and the poles of \( F(s) \) (real or complex conjugate)
Design problem: group together pole and zero pairs (pole-zero pairing): it affects the dynamic range and the sensitivity.

Unfortunately there are not general and consistent rules for the pole-zero pairing in order to minimize the sensitivity.

Two opposite approaches are suggested in the literature:
- Pair the high-Q poles with far away zeros
- Pair the high-Q poles with closed zeros

The only solution is to try different pairing and to compare them with Monte Carlo analysis.

For order > 6 the cascade design is inherently more sensitive to component variation than multiple-loop feedback realizations.
MULTIPLE LOOP FEEDBACK REALIZATIONS

Several topologies:

- Follow the leader feedback (FLF)
- Inverse follow the leader (IFLF)
- Generalize follow the leader feedback (GFLF)
- Primary resonator block (PRB)
- Leapfrog feedback (LF)
- Modified leapfrog feedback (MLF)
- Coupled biquad (CB)
- Minimum sensitivity feedback (MSF)
LEAPFROG TOPOLOGY

Simulate passive ladder networks, via signal flow graph

\[ I_0 = \frac{1}{R_s}(V_{in} - V_1) \]

\[ V_1 = \frac{1}{sC_1}(I_0 - I_2) \]

\[ I_2 = \frac{1}{sL_2}(V_1 - V_3) \]
If we multiply each current by an arbitrary resistance $R$, we define new “dummy” voltage variables

\[
V_0 = RI_0 \quad V_2 = RI_2 \quad V_4 = RI_4 \quad V_6 = RI_6
\]

\[
V_3 = \frac{1}{sC_3}(I_2 - I_4) \\
I_4 = \frac{1}{sL_4}(V_3 - V_5) \\
V_5 = \frac{1}{sC_5}(I_4 - I_6) \\
I_6 = \frac{1}{R_6}V_5 \\
V_{\text{out}} = V_5
\]
The equations become:

\[ V_0 = \frac{R}{R_s} (V_{in} - V_1) \]

\[ V_1 = \frac{1}{sRC_1} (V_0 - V_2) \]

\[ V_2 = \frac{R}{sL_2} (V_1 - V_3) \]

\[ V_3 = \frac{1}{sRC_3} (V_2 - V_4) \]

\[ V_4 = \frac{R}{sL_4} (V_3 - V_5) \]

\[ V_5 = \frac{1}{sRC_5} (V_4 - V_6) \]

\[ V_6 = \frac{R}{R_6} V_5 \]
The original set of equations and the modified one can be represented with the signal flow graphs:

![Signal Flow Graphs](image-url)
Scaling of the flow graph:

Variable transformation

Scaling by constants
The scaling of the flow graph is used in order to obtain realizable active implementations

- Inverting integrators
- Inverters
- Summators

Interconnection of second order loops ($R \approx R_s \approx R_6$)
The scaling is also useful for dynamic range optimization:

V₁ is too small
V₂ is too high

\[ V_1 \rightarrow K_1 V_1 \]
\[ V_2 \rightarrow V_1 / K_2 \]

**Result:** all the op-amp saturate (at different frequency) with the same input level.

- Perform a SPICE simulation of the active (or passive) network in order to determine the scaling factors.
If the passive prototype has transmission zeros at the finite (elliptic filters), it has the form (low pass).

Before to describe the network and sketch the flow diagram it is worth to remove the bridging capacitors $C_2$ and $C_4$ through the use of the Thevenin’s theorem.

\[ a_1 = \frac{C_2}{(C_1 + C_2)} \quad a_2 = \frac{C_2}{(C_3 + C_2)} \]
Similar modification follows if $C_4$ is removed

The equations concerning the state variables $V_1$, $V_3$ and $V_5$ change:

\[
V_1 = \frac{1}{sC'_1}(I_s - I_2) + \frac{V_3C_2}{C_1} \quad \quad C_1' = C_1 + C_2
\]

\[
V_3 = \frac{1}{sC'_3}(I_2 - I_4) + \frac{V_1C_2}{C_1 + C_3} + \frac{V_5C_4}{C_3 + C_4} \quad \quad C_3' = C_2 + C_3 + C_4
\]

\[
V_5 = \frac{1}{sC'_5}(I_4 - I_6) + \frac{V_3C_4}{C_5} \quad \quad C_5' = C_4 + C_5
\]
After scalings, aimed to the active realization:
SWITCHED CAPACITOR TECHNIQUE

- An active filter is made of op-amps, resistors and capacitors.

- The accuracy of the filter is determined by the accuracy of the realized time costants since the capacitors and resistors are realized by uncorrelated technological steps.

\[
\left(\frac{\delta \tau}{\tau}\right)^2 = \left(\frac{\delta R}{R}\right)^2 + \left(\frac{\delta C}{C}\right)^2
\]

- In CMOS technology \( \frac{\delta R}{R} \approx 40\% \); \( \frac{\delta C}{C} \approx 30\% \); hence \( \frac{\delta \tau}{\tau} \approx 50\% \), unacceptable for most of the applications.

- Hybrid realization with functional trimming.
Problems for a fully integrated realization

- Accuracy
- Values of capacitors and resistors: for 70 nm oxide thickness 1 pF -> 2000 µ²; 10 pF is a large capacitance. To get \( \tau = 10^{-4} \) sec \( R = 10^7 \Omega \)

The above problems are solved by the use of simulated resistors made of switches and capacitors.

MOS technology is suitable because:

- Offset free switches
- Good capacitors
- Satisfactory op-amps
Simple SC structures

\[ \Delta Q = C_1 (V_1 - V_2) \text{ every } \Delta t = T \]
\[ \Delta Q = i \Delta t = \frac{V_1 - V_2}{R} T \]

The two SC structures are (on average) equivalent to a resistor

\[ R_{eq} = \frac{T}{C_1} \]

If the SC structures are used to get an equivalent time constant \( \tau_{eq} = R_{eq} C_2 \) it results:

\[ \tau_{eq} = T \frac{C_2}{C_1} \]
• Its accuracy depends on the clock and on the capacitor matching accuracy
• If $\tau_{eq} = 40 T C_2 = 40 C_1$ (acceptable spread) regardless of the value of $\tau_{eq}$

**A more complex SC structure:**

$$\Delta Q = 2C_1(V_1 - V_2)$$

The charge is transferred twice per clock period $T$ or we assume as clock period half of the period of phases $\Phi_1$ and $\Phi_2$. 
Starting from the continuous-time circuit of the Integrator, we can obtain a SC integrator by replacing the continuous-time resistor with the equivalent resistances as follows:
We consider the samples of the input and of the output taken at the same times \( nT \) (the end of the sampling period).

- **Structure 1:**

  \[
  V_{out}[ (n+1)T ] = V_{out}(nT) - \frac{C_1}{C_2} V_{in}(nT)
  \]

  taking the z-transform:

  \[
  \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2} \cdot \frac{1}{z-1}
  \]

- **Structure 2:**

  \[
  V_{out}[ (n+1)T ] = V_{out}(nT) - \frac{C_1}{C_2} V_{in}(n+1)T
  \]

  taking the z-transform:
\[
\frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2} \cdot \frac{z}{z - 1}
\]

- **Structure 3:**

\[
V_{out}[(n+1)T] = V_{out}(nT) - \frac{C_1}{C_2} \{V_{in}[(n+1)T] + V_{in}(nT)\}
\]

taking the z-transform:

\[
\frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2} \cdot \frac{z + 1}{z - 1}
\]

Remember that for the continuous-time integrator:

\[
\frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{sR_1C_2}
\]

Comparing the sampled-data and continuous-time transfer functions we get:
• Structure 1:
  \[ R_1 \rightarrow \frac{T}{C_1} \quad s \rightarrow \frac{1}{T}(z - 1) \quad \text{FE approximation} \]

• Structure 2:
  \[ R_1 \rightarrow \frac{T}{C_1} \quad s \rightarrow \frac{1(z - 1)}{Tz} \quad \text{BE approximation} \]

• Structure 3:
  \[ R_1 \rightarrow \frac{T}{2C_1} \quad s \rightarrow \frac{2(z - 1)}{T(z + 1)} \quad \text{Bilinear approximation} \]

- It does not exist a simple SC integrator which implement the LD approximation.

- Note: the cascade of a FE integrator and a BE integrator is equivalent to the cascade of two LD integrators.
The key point is to introduce a full period delay from the input to the output.

The same result is got with:
STRAY INSENSITIVE STRUCTURE

The considered SC integrators are sensitive to parasitics.

**Toggle structure:**

- The top plate parasitic capacitance $C_{t,1}$ is in parallel with $C_1$
- It is not negligible with respect to $C_1$ and it is non linear
- The top plate parasitic capacitance $C_{t,1}$ acts as a toggle structure
**Bilinear resistor:**

- Both the parasitic capacitances $C_{t,1}$, $C_{b,1}$ act as toggle structures. Their values are different (of a factor $\approx 10$) and they are non-linear.
- Stray insensitivity can be got for the first two structures if one terminal is switched between points at the same voltage.
• The right-side parasitic capacitor is switched between the virtual ground and ground (note: even in DC $V_{v.g.}$ must equal $V_{ground}$)
• The left side capacitor is connected, during phase 1, to a voltage (or equivalent) source.
• The charge injected into virtual ground is important, not the one furnished by the input source.
• Structure A is equivalent to the toggle structure, but the injected charge has opposite sign.
• Equivalent negative resistance allows to implement non inverting integrators.
• It is possible to easily realize a stray insensitive bilinear resistor with fully differential configuration.
SC BIQUADRIC FILTERS

Consider a (continuous-time) biquadratic transfer function

$$H(s) = \frac{p_0 + sp_1 + s^2p_2}{s^2 + s\frac{\omega_0}{Q_0} + \omega_0^2}$$

If the bilinear transformation is applied, it results a z-biquadratic transfer function

$$H(s) = \frac{a_0 + za_1 + z^2a_2}{b_0 + zb_1 + z^2b_2}$$

where the coefficients are:

$$a_0 = p_0 - 2\frac{1}{T}p_1 + 4\frac{1}{T^2}p_2$$
\[ a_1 = 2p_0 - \frac{8}{T^2}p_2 \]

\[ a_2 = p_0 + \frac{2}{T}p_1 + \frac{4}{T^2}p_2 \]

\[ b_0 = \omega_0^2 - \frac{2\omega_0}{TQ} + \frac{4}{T^2} \]

\[ b_1 = 2\omega_0^2 - \frac{8}{T^2} \]

\[ b_2 = \omega_0^2 + \frac{2\omega_0}{TQ} + \frac{4}{T^2} \]
All the stable z-biquadratic transfer functions are realized by the topology:
Features:

- Loop of two integrators one inverting and the other noninverting.
- Damping around the loop provided by capacitor F or (and) capacitor E (usually only E or F are included in the network).
- Two outputs available \( V_{0,1}, V_{0,2} \).
- Denominator of the transfer function determined by the capacitors along the loop (A, B, C, D, E, F).
- Transmission zeros (numerator) realized by the capacitors (G, H, I, J).
- Input signal sampled during \( \Phi_1 \) and held for a full clock period.
- Charge injected into the virtual ground during \( \Phi_1 \).
Minimum switch configuration:
Charge conservation equations:

\[ DV_{0,1}(n+1) = DV_{0,1}(n) - GV_{\text{in}}(n+1) + HV_{\text{in}}(n) - CV_{0,2}(n+1) - E[V_{0,2}(n+1) - V_{0,2}(n)] \]

\[(B + F)V_{0,2}(n+1) = BV_{0,2}(n) + AV_{0,1}(n) - IV_{\text{in}}(n+1) + JV_{\text{in}}(n) \]

Taking the z-transform and solving, it results:

\[ H_1 = \frac{V_{0,1}}{V_{\text{in}}} = \frac{(IC + IE - GF - GB)z^2 + (FH + BH + BG - JC - JE - IE)z + (EJ - BH)}{(DB + DF)z^2 + (AC + AE - 2DB - DF)z + (DB - AE)} \]

\[ H_2 = \frac{V_{0,2}}{V_{\text{in}}} = \frac{Dlz^2 + (AG - DI - DJ)z + (DJ - AH)}{(DB + DF)z^2 + (AC + AE - 2DB - DF)z + (DB - AE)} \]

- 10 Capacitors
- 6 Equations \( a_0, a_1, a_2, b_0, b_1, b_2 \)
- Dynamic range optimization
• Scaling for minimum total capacitance in the groups of capacitors connected to the virtual ground of the op-amp₁ and the op-amp₂.

• Since there are 9 conditions, one capacitor can be set equal to zero

\[
E = 0 \quad \text{“F type”}
\]

\[
F = 0 \quad \text{“E type”}
\]

Firstly the 6 equations are satisfied. Later capacitors D and A are adjusted in order to optimize the dynamic range. Finally all the capacitor connected to the virtual ground of the op-amp are normalized to the smaller of the group.
Scaling for minimum total capacitance

Assume that $C_3$ is the smallest capacitance of the group. In order to make minimum the total capacitance $C_3$ must be reduced to the smallest value allowed by the technology ($C_{\text{min}}$)

- Multiply all the capacitors of the group by

$$k = \frac{C_{\text{min}}}{C_3}$$
- All these design steps can be performed with a suitable computer program

**Equivalences for input structures:**

![Diagram showing equivalences for input structures:](image)

- \( G-H \) for \( G>H \)
- \( H \) for \( G=H \)
- \( G \) for \( G<H \)
SC LADDER FILTERS

**Orchard’s observation**
Doubly-terminated LC ladder network that are designed to effect maximum power transfer from source to load over the filter passband feature very low sensitivities to value component variation.

**Syntesis of SC Ladder Filters:**

Symples approach
- Replace every resistance $R_i$ in an active ladder structure with a switched capacitor $C_i = T/R_i$.
- Use a full clock period delay along all the two integrator loop (it results automatically verified in single ended schemes).

It results an LD equivalent, except for the terminations.
**Quasi LD transformation:**

Prewarp the specifications using \( \sin(\omega T/2) \)

\[
\begin{align*}
\text{DESIRED SPECIFICATION} \\
\text{PREWARPED SPECIFICATION}
\end{align*}
\]
Effect of the terminations:

\[ H_{DI}(s) = \frac{R_3}{sC_2R_1R_3 + R_1} \]

if \( R_1 = \frac{T}{C_1} \) and \( R_3 = \frac{T}{C_3} \) we get:

\[ H_{DI}(s) = \frac{C_1}{sTC_2 + C_3} \]

\[ V_{out}(n + 1)(C_2 + C_3) = V_{out}(n)C_2 + C_1V_{in}(n) \]
Taking the z-transform we get: \[ zV_{\text{out}}(C_2 + C_3) = C_2 V_{\text{out}} + C_1 V_{\text{in}} \]

\[ H_{\text{DI}}(z) = \frac{C_1}{C_2(z - 1) + zC_3} = \frac{C_1 z^{-1/2}}{C_2(z^{1/2} - z^{-1/2}) + z^{1/2}C_3} \]

along the unity circle \( z = e^{j\omega_T} \)

\[ H_{\text{DI}}(e^{j\omega_T}) = \frac{C_1 e^{-j\omega_T/2}}{C_2(e^{j\omega_T/2} - e^{-j\omega_T/2}) + e^{j\omega_T/2}C_3} = \frac{C_1 e^{-j\omega_T/2}}{2j(C_2 + C_3) \sin \frac{\omega_T}{2} + C_3 \cos \frac{\omega_T}{2}} \]

The half clock period delay will be used in the cascaded integrator in order to get the LD transformation

- The termination is complex and frequency dependent.
- The integrating capacitor \( C_2 \) must be replaced by \( C_2 + C_3/2 \).
Complex termination:

Note: the output voltage changes during $\Phi$

$$V_{out}(n+1)C_2 = V_{out}(n)\frac{C_2^2}{C_2 + C_3} + C_1V_{in}(n)$$

Taking the z-transform:

$$zV_{out}C_2 = V_{out}\left(C_2 - \frac{C_2C_3}{C_2 + C_3}\right) + C_1V_{in}$$
The imaginary part of the contribution of the termination is negative.

The integrating capacitor $c_2$ must be replaced by $c_2 - \frac{1}{2} \frac{C_2 C_3}{C_2 + C_3}$.
Example: 5th order filter

Passive prototype

Flow diagram

SC implementation
EXACT DESIGN OF SC LADDER FILTERS

- A continuous-time network is exactly transformed into a sampled-data network through the mapping $z = \exp(sT)$.

- We can assume that an exact transformation is realized even through the LDI or the bilinear mapping, provided that the required pre-warping is made.

- The exact LD design of ladder filter is not possible because of the error given by terminations.

- The exact bilinear design is realizable through a suitable scaling.

Let us define the complex variables:

$$\gamma = \frac{1}{2}(z^{1/2} - z^{-1/2}) = \frac{1}{2}(e^{sT/2} - e^{-sT/2}) = \sinh\left(\frac{sT}{2}\right)$$

$$\mu = \frac{1}{2}(z^{1/2} + z^{-1/2}) = \frac{1}{2}(e^{sT/2} + e^{-sT/2}) = \cosh\left(\frac{sT}{2}\right)$$
\[
\lambda = \frac{z - 1}{z + 1} = \frac{z^{1/2} - z^{-1/2}}{z^{1/2} + z^{-1/2}} = \tanh \left( s \frac{T}{2} \right)
\]

They are related by the relationships:

\[
\lambda = \frac{\gamma}{\mu} \quad \mu^2 = 1 + \gamma^2 \quad z^{1/2} = \mu + \gamma
\]

Note: the \( \gamma \) plane is the LDI plane and the \( \lambda \) plane is the bilinear plane \((2/T\) normalized to 1\)

- To implement an exact LD equivalent \( s \) should be replaced by \( \gamma \)
- To implement an exact bilinear equivalent \( s \) should be replaced by \( \lambda \)
- Unfortunately, SC circuits having transfer function of the form \( 1/\lambda \) can not be realized in stray-insensitive form

- **Solution**: suitable scaling of the ladder network (or equivalently the flow diagram): if we divide all impedance of a network by the same scaling factor, the transfer function remains unchanged
Scaling of bilinear elements by $\mu$:

$$ R \rightarrow \frac{R}{\mu} $$

$$ \frac{1}{\lambda C} \rightarrow \frac{1}{\mu \lambda C} = \frac{1}{\gamma C} $$

$$ \lambda L \rightarrow \frac{\lambda L}{\mu} = \frac{\lambda \mu L}{\mu^2} = \frac{\gamma L}{1 + \gamma^2} = \frac{1}{\gamma L + \frac{\gamma}{L}} $$

Scaling changes:

- A resistor into a frequency dependent element
- A bilinear capacitor into an LD capacitor
- A bilinear inductance into parallel of $L$ - LD inductance with a $1/L$ - LD capacitor
Consider a 5th order elliptic filter (bilinear)

After scaling by $\mu$

F. Maloberti: Design of CMOS Analog Integrated Circuits - "Continuous Time and Switched Capacitor Filters"
After the elimination of the bridging capacitors

\[
C_1' = C_1 + C_2 + 1/L_2
\]

\[
C_3' = C_2 + C_3 + C_4 + 1/L_2 + 1/L_4
\]

\[
C_5' = C_4 + C_5 + 1/L_4
\]

\[
\alpha_1 = (C_2 + 1/L_2)/(C_1 + C_2 + 1/L_2) \quad \alpha_3 = (C_4 + 1/L_4)/(C_3 + C_4 + 1/L_4)
\]

\[
\alpha_2 = (C_2 + 1/L_2)/(C_3 + C_2 + 1/L_2) \quad \alpha_3 = (C_4 + 1/L_4)/(C_5 + C_4 + 1/L_4)
\]
The network is the same as an LD equivalent ladder filter with the exception of the frequency dependent terminations

\[
\gamma C_1(V_1 - \alpha_1 V_3) = \frac{\mu}{R_s} (V_{\text{in}} - V_1) - I_2
\]

\[
\gamma C_5(V_5 - \alpha_4 V_3) = I_4 - \frac{\mu}{R_L} V_5
\]

\[
V_1 = \frac{\frac{\mu}{R_s} V_{\text{in}} + \gamma \left( C_2 + \frac{1}{L_2} \right) V_3 - I_2}{\gamma C_1 + \frac{\mu}{R_s}}
\]

\[
V_5 = \frac{I_4 + \gamma \left( C_4 + \frac{1}{L_4} \right) V_3}{\gamma C_5 + \frac{\mu}{R_L}}
\]
After the dimensional scaling by $R$, ($\beta_s = R/R_s$, $\beta_e = R/R_L$)

$$V_1 = \frac{\beta_s \mu V_{in} + \gamma \tau_2 V_3 - V_2}{\gamma \tau_1 + \beta_s \mu}$$

$$V_5 = \frac{V_4 + \gamma \tau_4 V_3}{\gamma \tau_3 + \beta_e \mu}$$

If we remember the z-transfer function of the dumped integrator
\[ H_{DI}(z) = \frac{C_1 z^{-1/2}}{C_2(z^{1/2} - z^{-1/2}) + C_3 z^{1/2}} = \frac{C_1(\mu - \gamma)}{2C_2 \gamma + C_3(\gamma + \mu)} = \frac{C_1(\mu - \gamma)}{(2C_2 + C_3)\gamma + C_3\mu} \]

The denominators can be realized
The only design problem come from the input \( \beta_s \mu V_{in} \)

\[ \mu V_{in} = \frac{1}{2}(z^{1/2} - z^{-1/2})V_{in} \]

It is necessary to inject two samples per period T
Simple solution (stray sensitive)
Stray insensitive solution:

Use of a S/H:
SWITCHED CAPACITOR N-PATH FILTERS

- Narrow-band (high Q) filters cannot be realized with conventional design techniques.
- Required gain $A_0 \approx 200 \ Q_{\text{max}}$; $Q_{\text{pole}} \approx (\omega_0 + B/2)/2|\sigma|$

- Sensitivities to finite gain and capacitance variation proportional to $Q_{\text{max}}$
Solution with N-path circuits; are a number of identical low pass filters multiplexed at the input and the output.

Sampling period of the input signal: $T$; sampling period in each LP filter: $NT$
In the z-domain

\[ V_{\text{in}}^i(t) = \sum_{n = -\infty}^{+\infty} V_{\text{in}}(t) \delta(t - n\tau - iT) \]

\[ V_{\text{in, NP}}(t) = \sum_{i = 1}^{N} V_{\text{in}}^i(t) \]

\[ V_{\text{out, NP}}(t) = \sum_{i = 1}^{N} V_{\text{out}}^i(t) \]

\[ H_{\text{NP}}(z) = H_{\text{LP}}(z) \]
The z-transfer function of the N-path and the one of the low pass are the same, but the sampling frequencies are one N times the other

\[ z_{LP} = e^{s(NT)} = (e^{sT})^N = z^N \]

The N-path filter realizes the transformation

\[ z \rightarrow z^N \]

In the transfer function of the low pass filter.

- The gain requirement and the sensitivities are the one posed by the low-pass filter specifications

**Implementation:**

First order prototype:
Parallel implementation:

Note that the op-amp work only during a small period. They can be multiplexed.
In order to have same LP transfer function all the integrating capacitors $C^{(1)}$, $C^{(2)}$, ..., $C^{(n)}$ must be matched. This requirement is overcame with the analog RAM-type scheme.
Or better:

**Problem:**
Clock feedthrough noise appears at 1/T

**Solutions:**
- Pseudo N-path with circulating memory
- Use of high-pass prototype and $z \rightarrow z^{-N}$ transformations
FINITE GAIN AND BANDWIDTH EFFECT

If the op-amp has finite gain $A_0$ the “virtual ground” voltage is $V_0/A_0$

$$C_2 V_0(n+1) \left(1 + \frac{1}{A_0}\right) = C_2 V_0(n) \left(1 + \frac{1}{A_0}\right) - C_1 \left[V_{in}(n+1) + \frac{V_0(n+1)}{A_0}\right]$$

z-transforming:

$$H(z) = \frac{V_o(z)}{V_{in}(z)} = -\frac{C_1 z}{C_2 \left(1 + \frac{1}{A_0}\right)(z - 1) + \frac{C_1}{A_0}z}$$
Comparing $H(z)$ with the transfer function with $A_0 \to \infty$

$$H_{id}(z) = \frac{C_1 z}{C_2(z-1)}$$

$$H(z) = \frac{H_{id}(z)}{\left(1 + \frac{1}{A_0}\right) + \frac{C_1}{C_2 A_0} \frac{z}{z-1}} = \frac{H_{id}(z)}{\left(1 + \frac{1}{A_0}\right) + \frac{C_1}{C_2 A_0} \left(\frac{1}{z-1} + \frac{1}{2} + \frac{1}{2}\right)} = \frac{H_{id}(z)}{\left(1 + \frac{1}{A_0} + \frac{1}{2C_2 A_0}\right) + \frac{C_1}{2C_2 A_0} \frac{z-1}{z-1}}$$

Substituting $z = e^{sT}$, on the imaginary axis

$$H(e^{j\omega T}) = \frac{H_{id}(e^{j\omega T})}{1 + \frac{1}{A_0} + \frac{C_1}{2C_2 A_0} - j \frac{1}{2C_2 A_0} \tan(\omega T/2)} = \frac{H_{id}(e^{j\omega T})}{1 - m(\omega) - j \theta(\omega)}$$

Magnitude error $m(\omega) = -\frac{1}{A_0} \left(1 + \frac{C_1}{2C_2}\right)$

Phase error $\theta(\omega) = \frac{C_1}{2C_2 A_0 \tan(\omega T/2)} \approx \frac{C_1}{C_2 A_0 \omega T}$
For the noninverting integrator

\[
C_2 V_0(n + 1) \left(1 + \frac{1}{A_0}\right) = C_2 V_0(n) \left(1 + \frac{1}{A_0}\right) + C_1 \left[ V_{\text{in}}(n) + \frac{V_0(n + 1)}{A_0} \right]
\]

z-transforming and solving

\[
H(z) = \frac{V_0(z)}{V_{\text{in}}(z)} = \frac{C_1}{C_2 \left(1 + \frac{1}{A_0}\right)(z - 1) + \frac{C_1}{A_0}z}
\]

Same magnitude and phase error result
**Effect of the finite bandwidth:**

\[ \tau = \frac{1}{\omega_0} \]

\[ \tau_1 = \tau \frac{C_1 + C_2}{C_2} = 10 \]
Since the charge is injected when the capacitor $C_1$ is connected to the virtual ground, during this phase the output will display a considerable transient.

During the phase when $C_1$ is disconnected a residual transient is performed by the output. This transient does not correspond to any charge transfer into $C_2$ (of course).

If $T/2$ is comparable with $\tau_1$ or $\tau_2$ we have two effects:

1. Incomplete charge transfer
2. Virtual ground voltage shift, which totally (in real situations) disappears during the successive half clock period
• If we sample the output during $\Phi_2$ we have only a magnitude error
• If we sample the output during $\Phi_1$ we have an additional voltage error that will be “forgotten”. It corresponds to a phase error

**For inverting and non inverting integrators:**

$$m(\omega) = e^{-\frac{C_2}{C_1 + C_2} \frac{\omega_0 T}{2}} \left[ 1 - \frac{C_2}{C_1 + C_2} \cos \omega T \right]$$

$$\theta(\omega) = e^{-\frac{C_2}{C_1 + C_2} \frac{\omega_0 T}{2}} \sin \omega T$$
Reduction of the finite gain effect:

- The effect of the finite gain can be reduced with techniques based on principles that similar to the autozero used in comparators.

- The virtual ground voltage must be sampled and held without changing the output voltage.
During the S/H of the virtual ground voltage the integrating capacitor must be disconnected in order to preserve its stored charge.

A simple unity gain closed loop connection destroys the output dependent virtual ground voltage.

A slave capacitor $C_s$ previously charged to the output voltage helps in solving the problem.
The output voltage changes only of the global offset (if $C_s$ is not required to integrate charge during $\Phi_2$)

**Three solutions:**

- $C_s$ is required to discharge the injecting capacitor $C_1$ to the global input offset.
- $C_s$ is required to discharge an extra-capacitor $C_2$, which, during $\Phi_1$ acts as a battery, creating a virtual ground at the node N.
The slave capacitor $C_s$ is precharged at $(V_{out} - V_{in})$. During $\Phi_2$ if $C_1 = C_s$ the charge redistribution between $C_1$ and $C_s$ is such that $V_{out}$ does not change.

**Notes:**

- The parasitic capacitance of the node A acts as a toggle SC which inject charge into the small $C_s$ during $\Phi_2$.
- Only inverting integrator
• Magnitude error is reflected into a frequency error
• Phase error is reflected into a Q error

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Magnitude error</th>
<th>Phase error</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>++</td>
<td>=</td>
</tr>
<tr>
<td>#2</td>
<td>=</td>
<td>+</td>
</tr>
<tr>
<td>#3</td>
<td>=</td>
<td>++</td>
</tr>
</tbody>
</table>

Same circuit solutions can be applied do SC amplifiers and converters.
FULLY DIFFERENTIAL CIRCUITS

- Fully differential configurations reduce the clock feedthrough noise and increase the dynamic range.
- They allow an increase design flexibility

Simple integrator (inverting and non inverting)
Immediate sampling (inverting and non inverting) integrator:

![Immediate sampling integrator diagram]

Delayed sampling (inverting and non inverting) integrator:

![Delayed sampling integrator diagram]
It is possible to reduce the op-amp finite bandwidth dependence by the use of delayed sampling inverting and non-inverting integrators along a second order loop.
The peaking in the frequency response due to the phase error is strongly reduced.

It is easy to realize bilinear integrators.
LAYOUT CONSIDERATIONS IN SC CIRCUITS

A SC circuit is the interconnection of
  • Op-amp
  • Switches
  • Capacitors

We have different lines of interconnections:
  • Signal
  • Bias
  • Clock

General rules:
  • Separate as far as possible, clock lines and signal lines
  • Top plate of capacitors connected to virtual ground
  • Maximum area switch and, when possible, only one transistor to realize the switch (minimum clock feedthrough)
FLOOR PLANING FOR SINGLE ENDED CIRCUITS

- Choose the dimension of the capacitor’s array in order to fit the op-amps dimension
- Input and output of the op-amps in the proper position
FLOOR PLANING FOR DIFFERENTIAL CIRCUITS
SWITCHES LAYOUT

CAPACITOR LAYOUT

- Use parallel connection of unity capacitors
- The residual capacitance must have the same perimeter/area ratio as the unity capacitors
- Common centroid only if is effectively necessary
NOISE IN SC CIRCUITS

The noise sources in a SC network are:

- Clock feedthrough noise
- Noise coupled from power supply lines and substrate
- kT/C noise
- Noise generators of the op-amp

The first two sources are the same as in mixed analog-digital circuits.

*kT/C noise:*

Consider the simple network:

In the “on” state the switch can be modeled with a noisy resistor
Noise equivalent circuit:

The white spectrum of the “on” resistance is shaped by the low pass action of the $R_{on}C$ filter. The noise voltage across the capacitor $C$ has spectrum:

$$S_{n,c} = \overline{v_{n,c}^2} = 4kTR_{on}|H(f)|^2\Delta f = \frac{4kTR_{on}\Delta f}{1 + (2\pi fR_{on}C)^2}$$
When the switch is turned “off” the noise voltage $v_{n,c}$ is sampled and held onto $C$.

The folding of the spectrum in band-base gives a white spectrum.
It power (the dashed area) is equal to the integral of $S_{n,c}$

$$
\overline{v_{n,c}^2} = \int_0^\infty \frac{4kTR_{on}\Delta f}{1 + (2\pi fR_{on}C)^2} df = \frac{4kT}{2\pi C} (\text{atan} x)_{\infty} = \frac{kT}{C}
$$

**Procedure for the noise calculation in SC networks:**

- Assume all the noise sources uncorrelated
- Neglect the direct coupling input-output
- Consider, in the sampled-data domain, the contribution to the output of each noise source (SC structures + op-amps)
- Superpose quadratically all the contributions
Low-frequency noise reduction techniques:

- Chopper-stabilization technique
- Correlated double sampling