# Design of Analog Integrated Circuits

# A/D and D/A Converters

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# OUTLINE

- A/D Conversion Fundamentals
- A/D Converter Characteristics
- Nyquist-rate A/D Converters
- Oversampled A/D Converters
- D/A Converters
- Limits and Final Considerations

# A/D Conversion Fundamentals

- A/D converters accomplish two key operations: sampling and quantization

- Sampling ➜ $x^*(nT_s) = \sum_{n=-\infty}^{\infty} x(t)\delta(t - nT_s)$

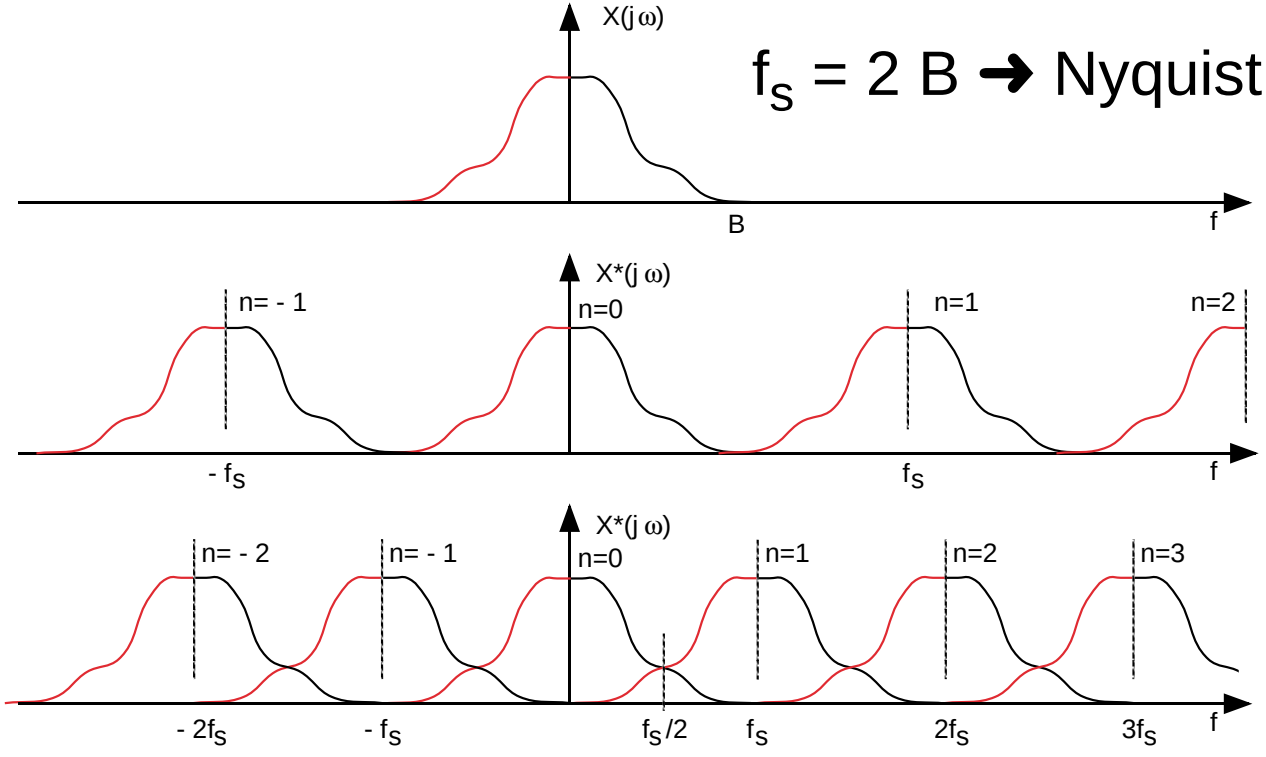
- The output of an ideal sampler is a series of delta functions weighted by the input x(nT)

- The spectrum of the sampled signal x* is

$$X^*(s) = \sum_{n=-\infty}^{\infty} x(nT_s)e^{-snT_s} = \frac{1}{T_s}\sum_{n=-\infty}^{\infty} X(s - jn\omega_s)$$

# A/D Conversion Fundamentals

- X(s) is the spectrum of the continuous-time signal x(t)
  - ➥ Aliasing ➜ Anti-aliasing filter




$f_s = 2\,B$ ➜ Nyquist Frequency

# A/D Conversion Fundamentals

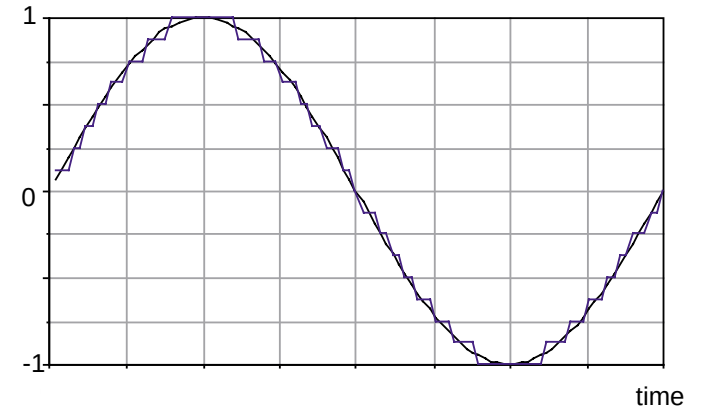
- Quantization ➜ The number of bits N of the digital code is finite
  - ➥ N-bits ➜ $2^N$ codes, each code represents a quantization level
- The amplitude of the constant spacing between quantization levels is $\Delta = V_{fs} / 2^N$ (where $V_{fs}$ is the full-scale amplitude and $\Delta$ is the quantization step)
  - ➥ For example, a 10-bit converter with full-scale amplitude equal to 1.023 V encodes the analog input with 1 mV discretization
  - ➥ If the input voltage is 624.8 mV, the digital output corresponds to the closer quantization level ➜ 624.5 mV
  - ➥ Since the quantization level is not equal to the input voltage, an error affects the output (0.3 mV in the example)

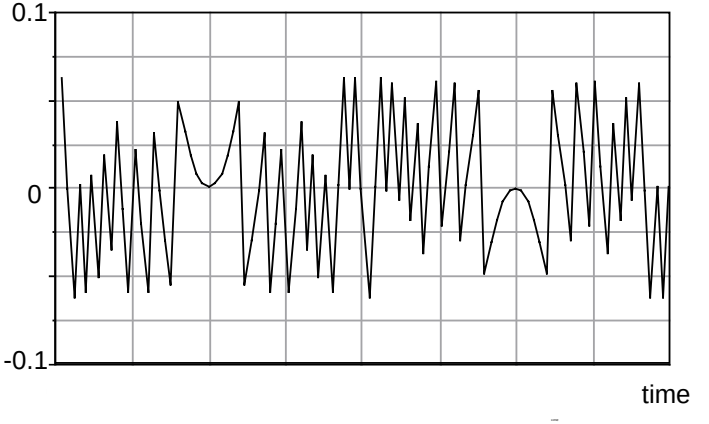
# A/D Conversion Fundamentals

- The error due to the quantization process is called quantization error $\varepsilon_Q$ ➜ $-\Delta / 2 < \varepsilon_Q < \Delta / 2$
- The quantization error represent an inherent limit of any data converter ➜ The quantization error is zero only if the number of bits of the digital code is infinite
- The quantization error is a consequence (and a measure) of the finite A/D converter resolution
- In an analog system the dynamic range performance is measured by the Signal-to-Noise Ratio (SNR) ➜ It is useful to define the converter resolution in terms of SNR (in addition to the number of bits)

# Is Quantization Error Noise?

- Quantization error can be considered a noise if
  - All quantization levels occur with equal probability
  - The quantization steps are uniform
  - The quantization error is not correlated with the input signal
  - A large number of quantization levels are used
- In many practical situations the above rules are not strictly fulfilled (for example Sigma-Delta Modulators)

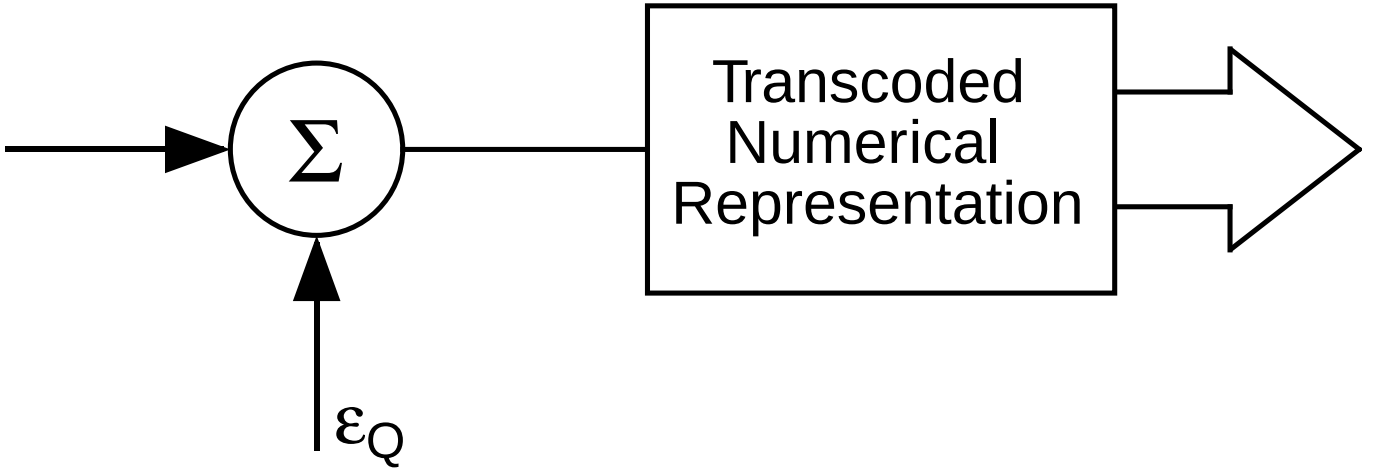


# Features of the Quantization Noise

- The quantization error is limited to the interval $-\Delta / 2 < \varepsilon_Q < \Delta / 2$
  - The probability distribution function of $\varepsilon_Q$, $p(\varepsilon_Q)$, is assumed constant

$$p(\varepsilon_Q) = \frac{1}{\Delta} \text{ for } \varepsilon_Q \in \left[-\frac{\Delta}{2}, \frac{\Delta}{2}\right]; \quad p(\varepsilon_Q) = 0 \quad \text{otherwhise}$$



# FEATURES OF THE QUANTIZATION NOISE

- Power ➜ The power for the quantization noise $P_Q$ is

$$P_Q = \int_{-\infty}^{\infty} \varepsilon_Q^2 p(\varepsilon_Q) d\varepsilon_Q = \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} \frac{\varepsilon_Q^2}{\Delta} d\varepsilon_Q = \frac{\Delta^2}{12}$$

- Sine wave with amplitude $V_{fs} / 2$ ➜ Power $V_{fs}^2 / 8$

$$SNR = 10Log\frac{P_{sig}}{P_{\varepsilon_Q}} = \frac{V_{fs}^2/8}{[V_{fs}/(2^N - 1)]^2/12} \cong 6.02N + 1.76 \ [dB]$$

# FEATURES OF THE QUANTIZATION NOISE

- Triangular wave with amplitude $V_{fs}$ / 2 ➜ Power $V_{fs}^2$ / 12

$$SNR = \frac{V_{fs}^2/12}{[V_{fs}/(2^N - 1)]^2/12} \cong 6.02N \quad [dB]$$

- Effective number of bits $N_{eff}$

$$N_{eff,sin} = \frac{SNR_{dB} - 1.76}{6.02}$$

$$N_{eff,tr} = \frac{SNR_{dB}}{6.02}$$

# FEATURES OF THE QUANTIZATION NOISE

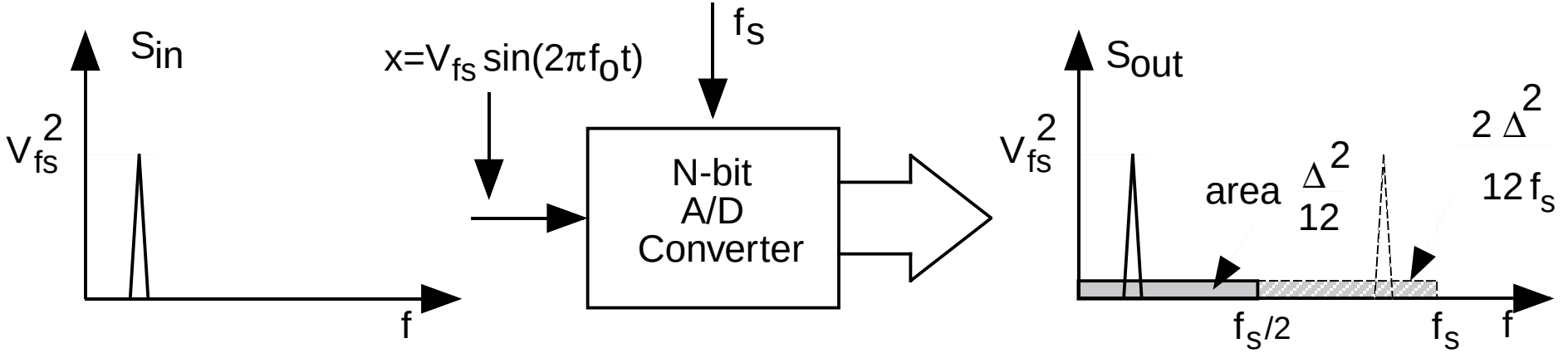
- Power spectrum ➜ Shows in which way the noise power is distributed over the Nyquist interval
  - The power spectrum is the Laplace transform of the autocorrelation function $R_\varepsilon(\tau)$ of $\varepsilon_Q$

$$P_\varepsilon(f) = \int_{-\infty}^{\infty} R_\varepsilon(\tau) e^{-j2\pi f\tau} d\tau$$

- The autocorrelation function of the noise is difficult to express
  - Successive quantization error samples are weakly correlated
  - The autocorrelation $R_\varepsilon(\tau)$ almost vanishes for $-T_s > \tau > T_s$

# FEATURES OF THE QUANTIZATION NOISE

- The quantization noise is an additive white noise
  - Power ➜ $\Delta^2 / 12$, uniformly spread over the Nyquist band
  - Power spectral density ➜ $2\,\Delta^2 / 12\,f_s$

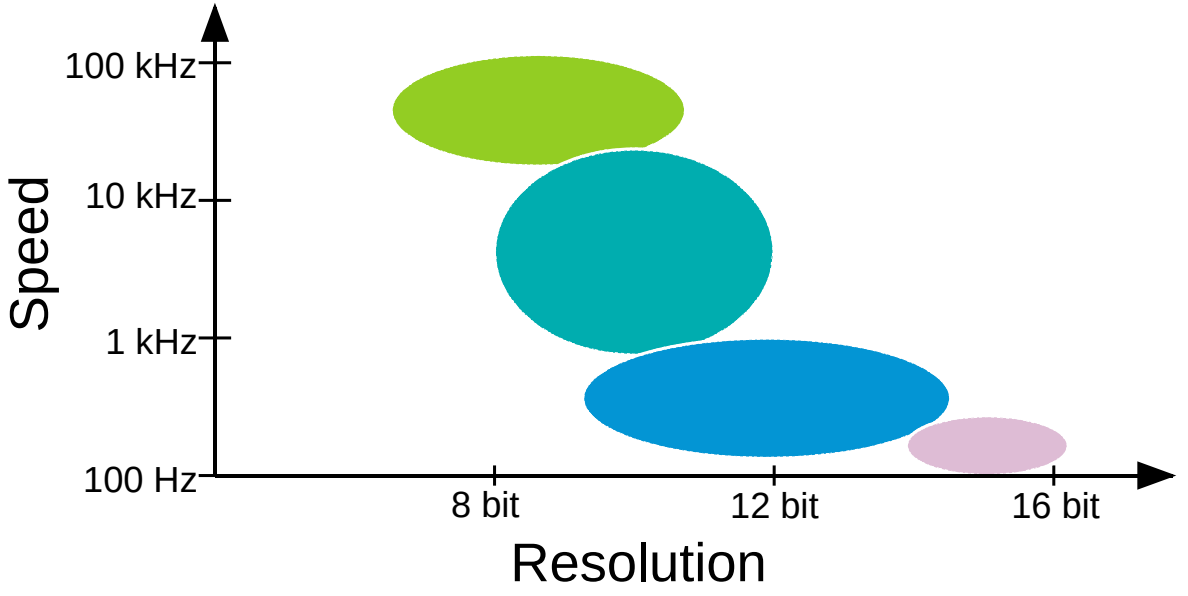



Input Spectrum

Output Spectrum

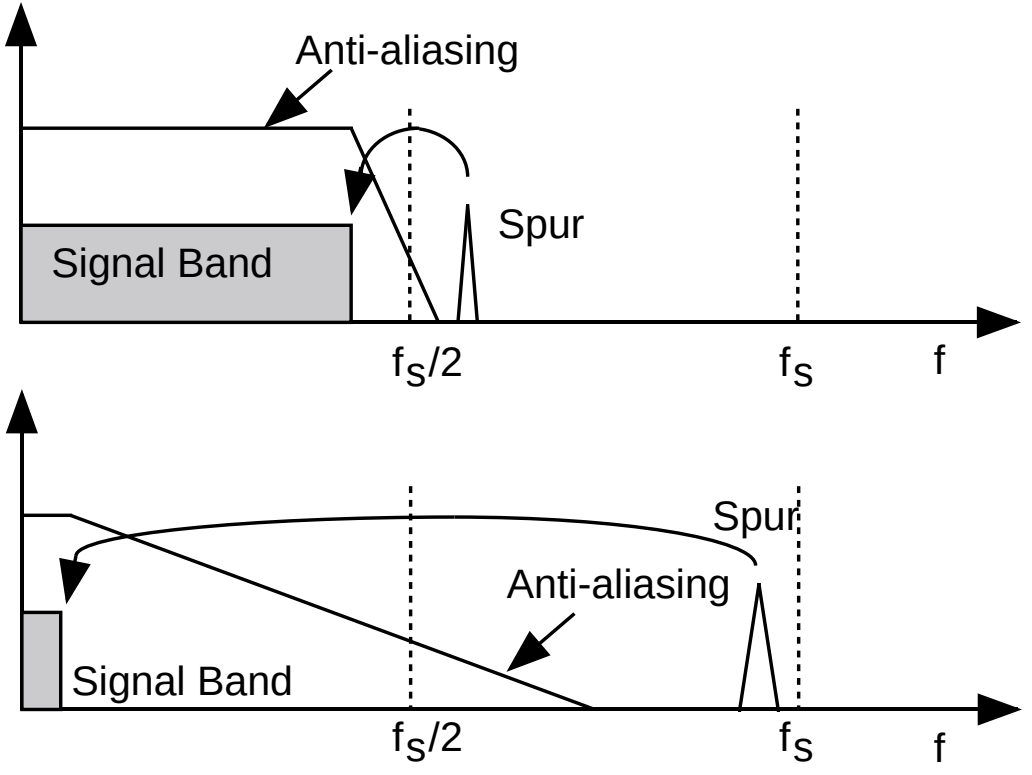
# A/D Converter Architectures

- Different A/D converter architectures either Nyquist rate and oversampled
  - ➥ Trade-off between speed and resolution
  - ➥ Application dependent




# NYQUIST RATE VS OVERSAMPLED CONVERTERS

- Anti-aliasing filter ➜ Significantly attenuate spurs while preserving the signal band

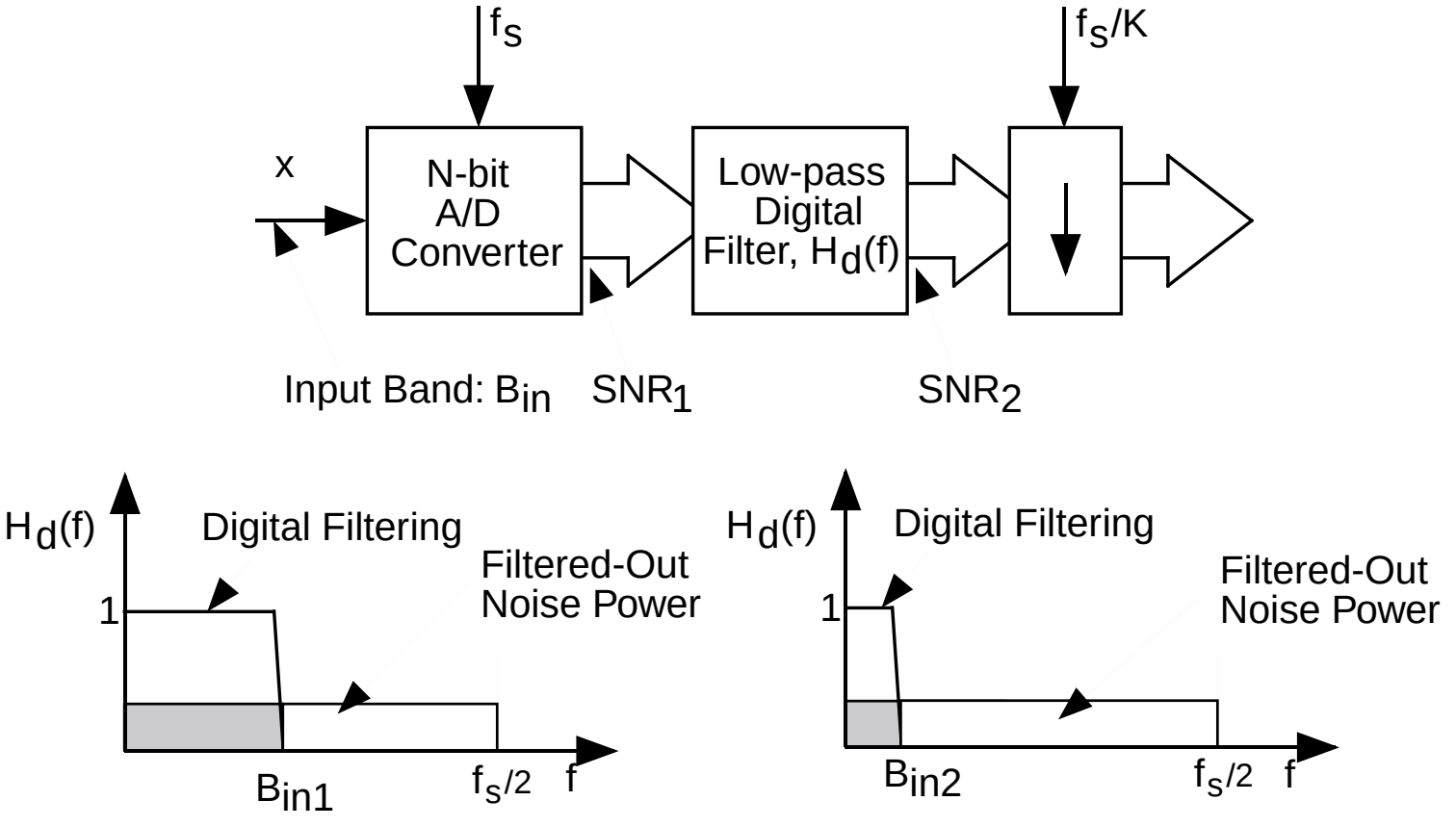


# NYQUIST RATE VS OVERSAMPLED CONVERTERS

- In Nyquist rate converters the signal band occupies almost the entire Nyquist interval ➜ The entire quantization noise power affects the signal
- In oversampled converters the signal band occupies only a fraction of the Nyquist interval ➜ Only part of the quantization noise power affects the signal
- The SNR can be improved by filtering in the digital domain the out-of-band quantization noise
- The cost that we have to pay is an additional digital filter and analog operation at high speed

# ADVANTAGES OF OVERSAMPLING

- Oversampling trades speed with resolution



# ADVANTAGES OF OVERSAMPLING

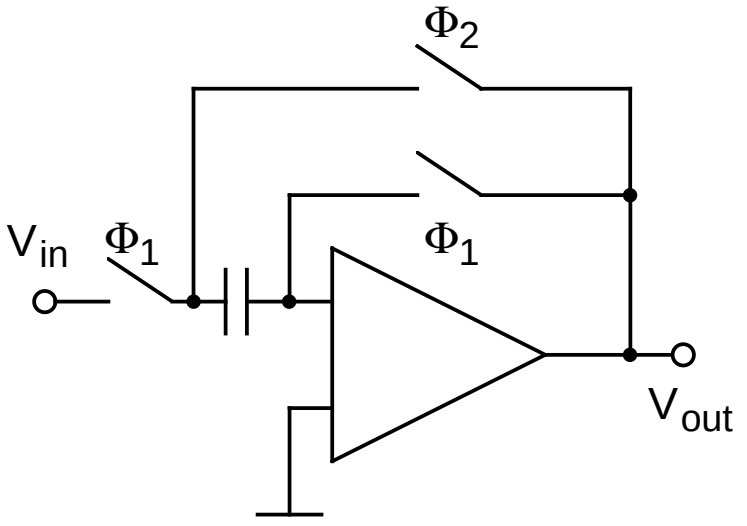
- Doubling the sampling frequency (oversampling) ➜ The in band noise power becomes half
  - ☺ SNR grows by 3 dB
  - ☺ The effective number of bits increases by 0.5
  - ☹ For gaining one bit of resolution it is necessary to increase the sampling by a factor 4
  - ☹ For increasing the resolution, for example, by 5 bits the sampling frequency should be multiplied by 1024!
- Oversampling by itself is not a convenient technique for enhancing resolution ➜ To achieve substantial benefits, we have to use also noise shaping

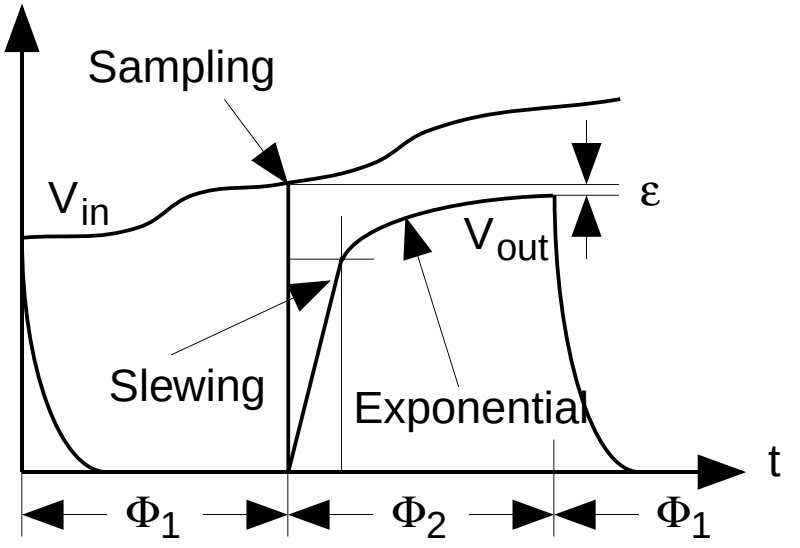
# A/D Converter Characteristics

- The key features characterizing an A/D converter are speed and accuracy
- The conversion rate quantifies the speed ➜ It is measured in Hertz or in samples per second (S/s)
- The number of bits or the SNR (expressed in dB) are the parameters normally used to quantify the accuracy or the resolution
- Alternatively, accuracy can be expressed as a fraction of the full-scale signal ➜ It is expressed in parts-per-million (ppm)
- Many effects influence both the dynamic and the static behavior

# SPEED CHARACTERISTICS

- The maximum sampling rate achieved by a converter is related to the time required for completing the specific processing functions
- Example ➜ Sample and hold with real operational amplifier



# SLEW RATE AND BANDWIDTH

- The non-linear response results from the following equations

$$\begin{cases} V_{out}(t) = SRt & \text{for } t \le t_{sl} \\ V_{out}(t_{sl}) = SR \cdot t_{sl} = V_{in} - V_{lin} & \text{for } t = t_{sl} \\ V_{out}(t) = (V_{in} - V_{lin})e^{-(t-t_{sl})\tau} & \text{for } t > t_{sl} \end{cases}$$

  - SR ➜ slew-rate, $V_{lin}$ ➜ linear range, $\tau$ ➜ time constant (bandwidth) and $T_S$ ➜ sampling period

- The slewing time must be a small fraction of $T_S$
- The bandwidth of the amplifier must be high enough to allow a suitable number of time constants for the exponential settling

# CLOCK JITTER

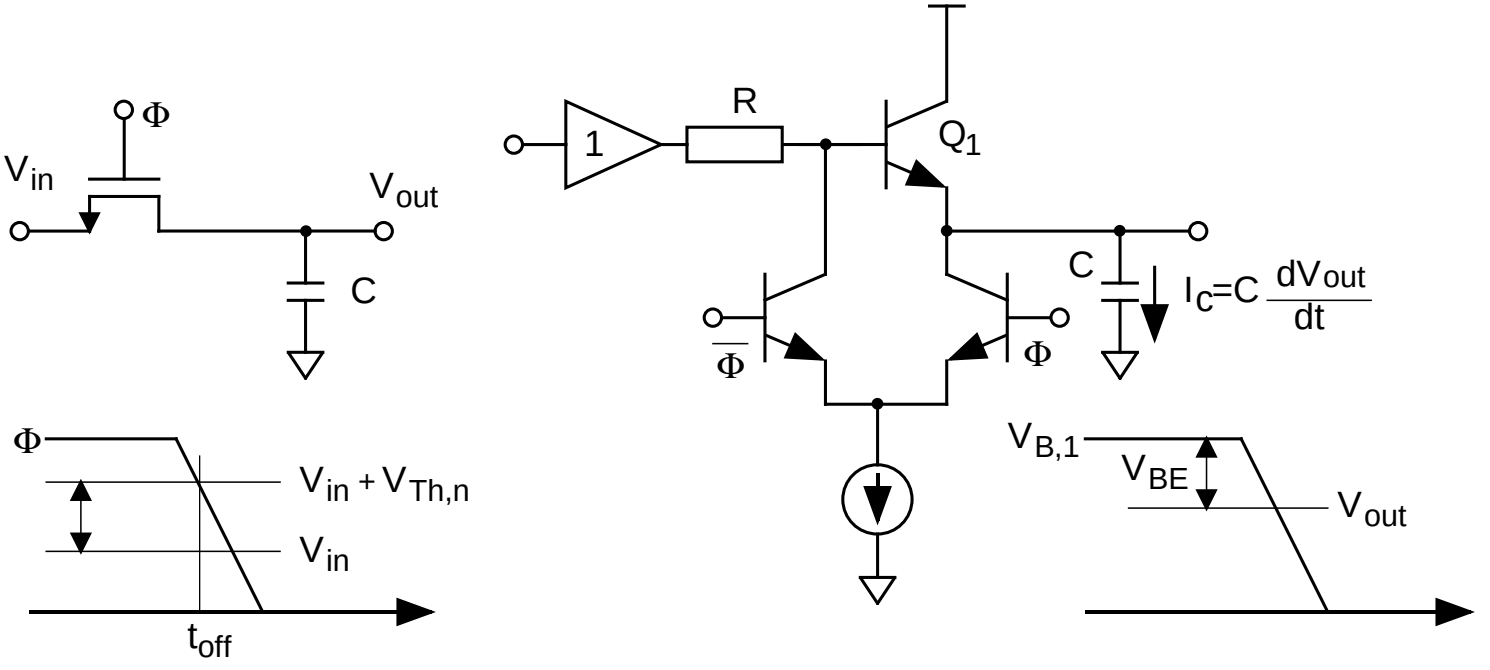
- Sampling clock jitter ➜ If the command used for opening the sampling switch is affected by jitter, the sampling is not uniform
- The effect can be described as a noise source ➜ Jitter noise $\varepsilon_{ji}$
- The effect of $\varepsilon_{ji}$ can be estimated by considering the sampling of a sinusoidal signal

  $$\varepsilon_{ji} = A\{\sin[\omega_{in}(nT + \delta_{ji})] - \sin[\omega_{in}nT]\} = \delta_{ji}A\omega_{in}\cos(\omega_{in}nT)$$

- The error is relevant when the associated power $(A\,\delta_{ji}\,\omega_{in})^2 / 8$ becomes comparable to the quantization noise
- The limit is achieved when $(\delta_{ji}\,\omega_{in})^{-2}$ approaches the SNR

# APERTURE DISTORTION

- Aperture distortion ➜ The sampling instants depends on the input amplitude since the exact instant of sampling occurs when the switch disconnects the input from the storing element



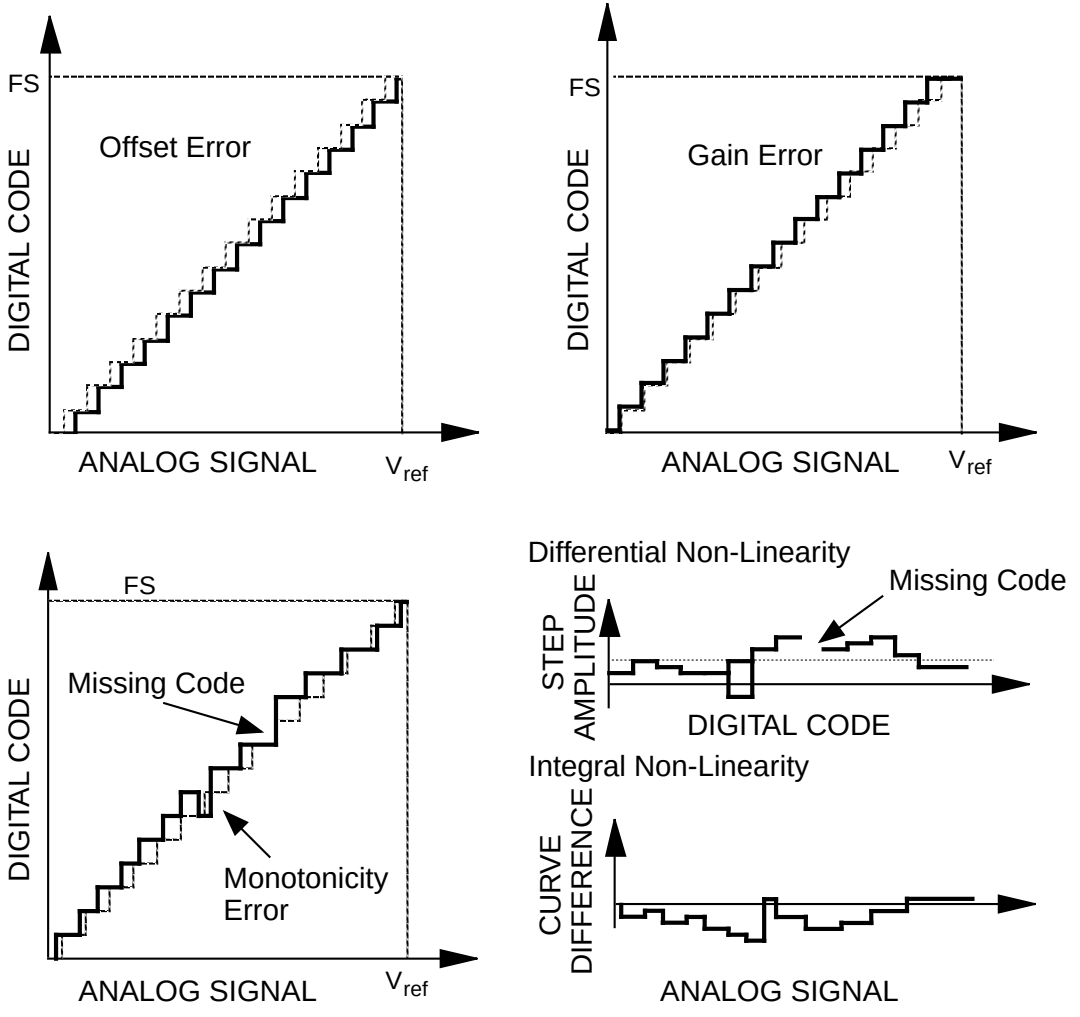
# APERTURE DISTORTION

- The aperture distortion describes the dependence of the sampling instants on the input amplitude
- At very high frequency the use of MOS switches becomes problematic when also high resolution is required
  - The finite on-resistance of the switch $R_{on}$ and the sampling capacitor C lead to a time constant that affects the tracking of the input
  - $R_{on} = L / [ W C_{ox} \mu (V_{GS} - V_{Th} - V_{DS})]$
  - The on-resistance of a minimum area n-channel transistor operating with 1 V overdrive and a negligible $V_{DS}$ is as high as 10 kΩ ($t_{ox}$ = 15 nm, $\mu_n$ = 520 $cm^2$ / V s) ➜ With a sampling capacitance of 1 pF the time constant becomes 10 ns

# RESOLUTION CHARACTERISTICS

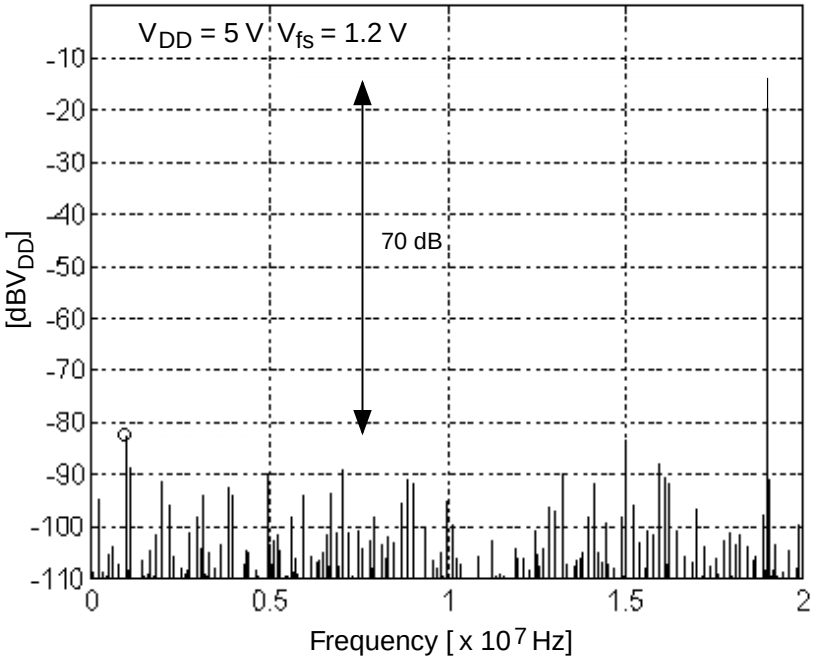
- An A/D converter never reaches the theoretical SNR corresponding to the desired number of bits
  - Various static or dynamic errors determine extra noise that, in turn, deteriorates the output accuracy
- Imperfections affecting the static behavior
  - The input-output transfer characteristic represents the digital output code as a function of the analog input signal
  - Ideally the input-output transfer characteristic of an A/D converter is a $2^N$ step staircase with uniform step amplitude
  - Errors in the transfer characteristic ➜ Offset error, gain error, monotonicity error, missing code error, differential linearity error, integral linearity error

# STATIC ERRORS



# NON LINEARITY ERRORS

- The integral non-linearity represents a distortion of the input-output transfer characteristic and leads to harmonic distortion, degrading the spurious free dynamic range



# NYQUIST RATE A/D CONVERTERS

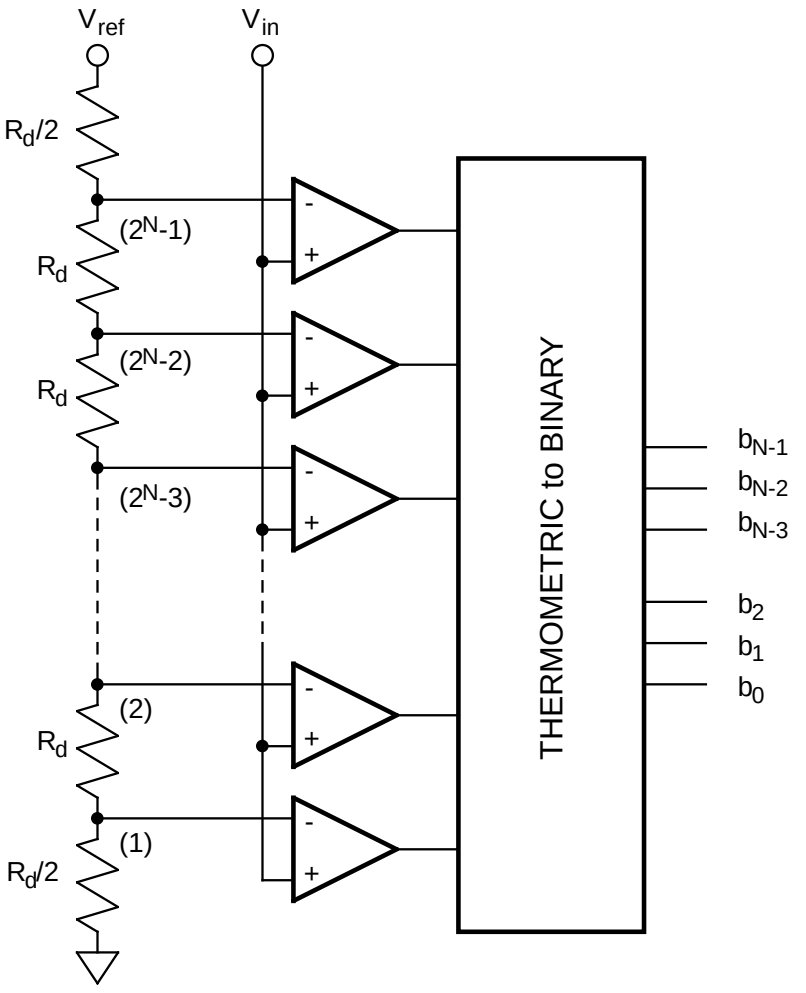
- High speed and low-resolution A/D converters
- The sampling frequency used in Nyquist-rate converters is close to the highest possible limit allowed by the technology
- The trend in signal processing systems is to place A/D converters as close as possible to the analog input
  - ➥ Most of the processing is performed in the digital domain
  - ☺ Advantage ➜ Flexibility (the system can be reconfigured just by changing the software)
  - ☹ Problem ➜ Large band systems (telecommunications) require both high speed of operation and high resolution

# NYQUIST RATE ARCHITECTURES

- Full flash A/D converters
- Two-step flash A/D converters
- Folding A/D converters
- Successive approximation A/D converters
- Interleaved A/D converters
- Pipeline A/D converters

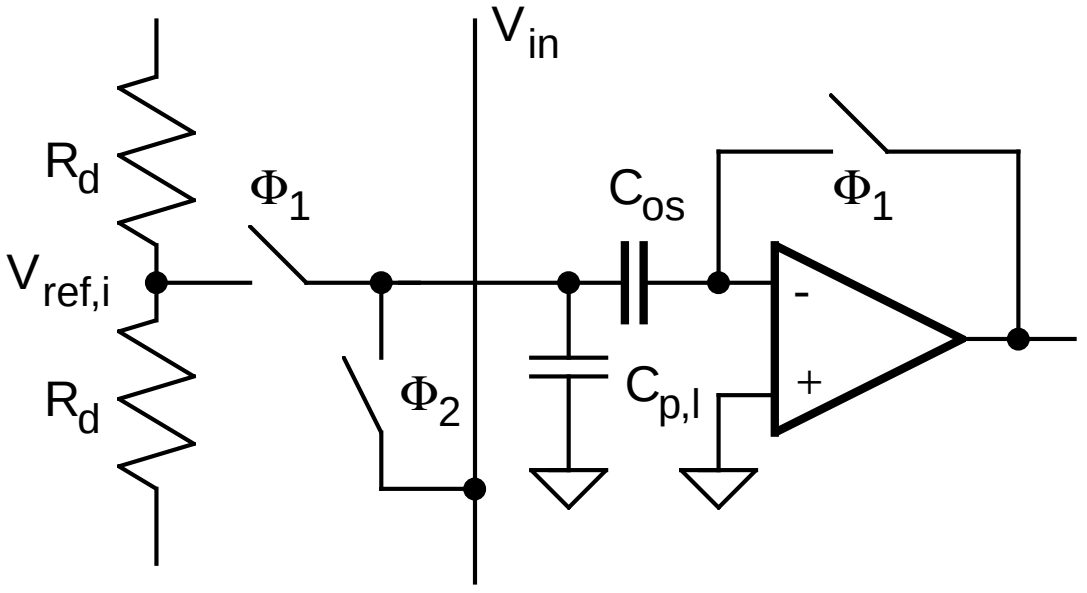
# FULL FLASH A/D CONVERTERS

- Thermometric coding
- Resistive string to achieve the quantization voltages required
- An N-bit converter requires
  - ➥ $2^N$ series resistors
  - ➥ $2^N - 1$ comparators
- Conversion time ➜ One clock cycle



# FULL FLASH A/D CONVERTERS

- Limits to accuracy
  - ☹ Matching between integrated resistors
  - ☹ Comparator offset
  - ☹ Loading impedance of each tap of the resistive string

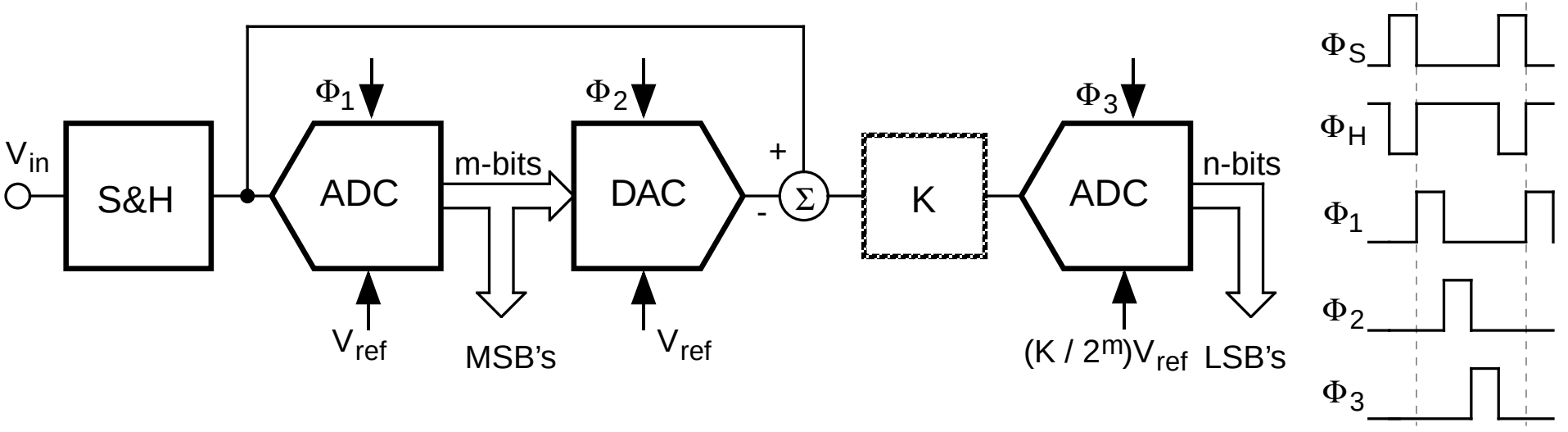


# FULL FLASH A/D CONVERTERS

- An inherent limitation of the full flash architecture comes from the exhaustive approach used
- N bit of resolution require $2^N - 1$ comparators
  - ☹ The complexity of the circuit increases exponentially with the number of bits and the chip area and the power consumption become unacceptable
  - ☹ The load at the input terminal increases exponentially with the number of bits
- Suitable for very high speed, low resolution A/D converters (for example for video applications)

# TWO-STEP FLASH A/D CONVERTERS

- The advantage of the full flash method vanishes when the number of bits exceeds 8 or 9
- Two-step flash A/D converter ➜ Coarse conversion followed by a fine conversion



# TWO-STEP FLASH A/D CONVERTERS

- The achieved resolution is N = m + n
- If the subtraction and the amplification by the factor K do not require additional clock cycles, the conversion time is two clock cycles
- The two-step flash architecture requires two full flash A/D converters, a D/A converter and a subtracting amplifier
- The number of comparators required is significantly reduced with respect to the full flash architecture ➜ Only $(2^m + 2^n - 2)$ instead of $2^{n+m}$

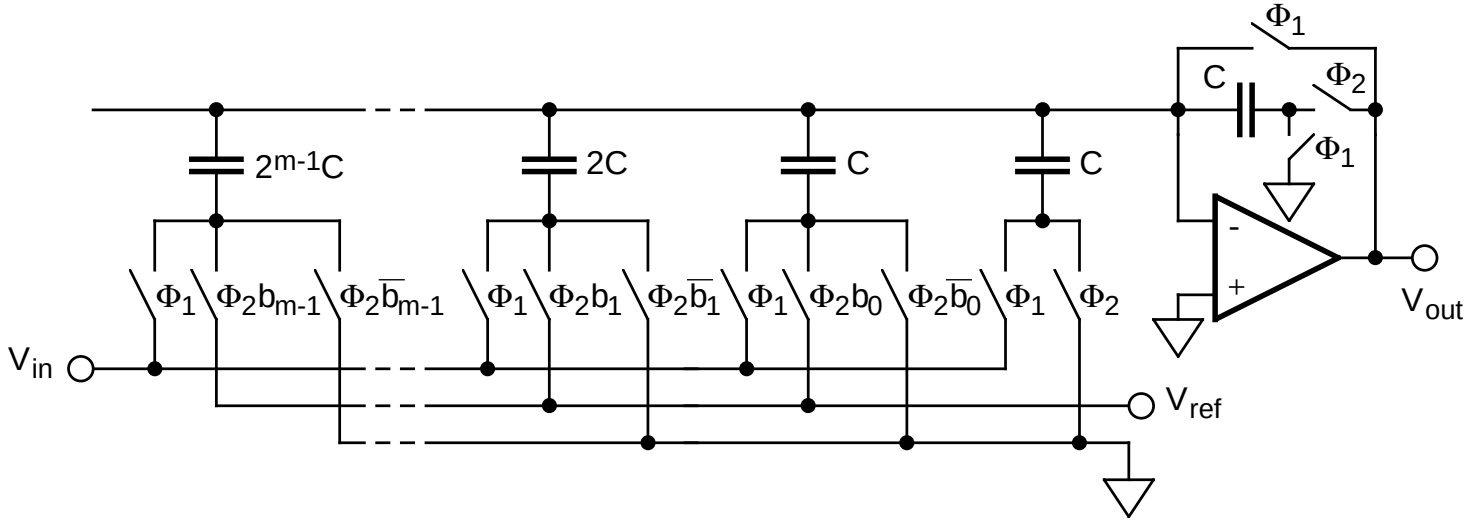
# TWO-STEP FLASH A/D CONVERTERS

- Two-step flash A/D converter limitations
  - ☹ The subtracting amplifier can be the real limit to speed, since subtraction and amplification must settle within half of a quantization step, thus requiring time
  - ☹ Successive samples are weakly correlated ➜ The subtracting amplifier must ensure large output swing within the subtracting period
  - ☹ Typically an additional clock cycle for the subtraction and amplification operation is required
  - ☹ The mismatch between the coarse and fine reference voltages or an error in the multiplying factor degrade the linearity

# TWO-STEP FLASH A/D CONVERTERS

- Example ➜ Switched capacitor circuit which incorporates DAC, subtractor and multiplier by a factor $2^m$ ($B = b_{m-1}, \ldots, b_0$)

$$V_{out} = 2^m V_{in} - \sum_{i=0}^{m-1} V_{ref} 2^i b_i = 2^m \left[ V_{in} - V_{ref} \frac{B}{2^m} \right]$$

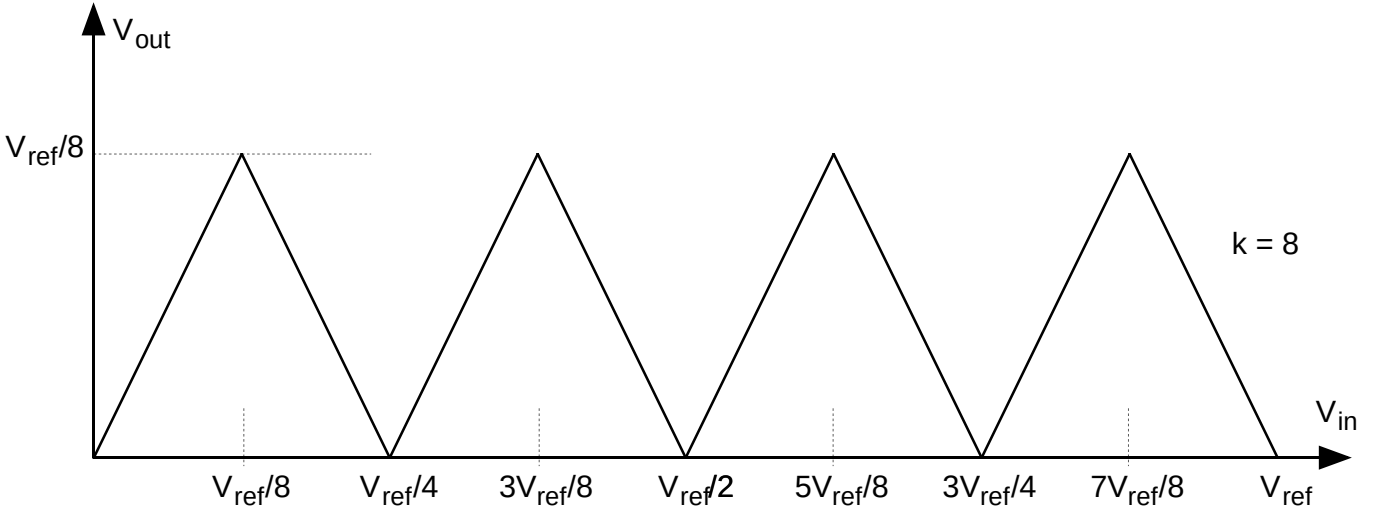


# FOLDING A/D CONVERTERS

- The folding technique is based on a non-linear preprocessing of the input signal before the A/D conversion

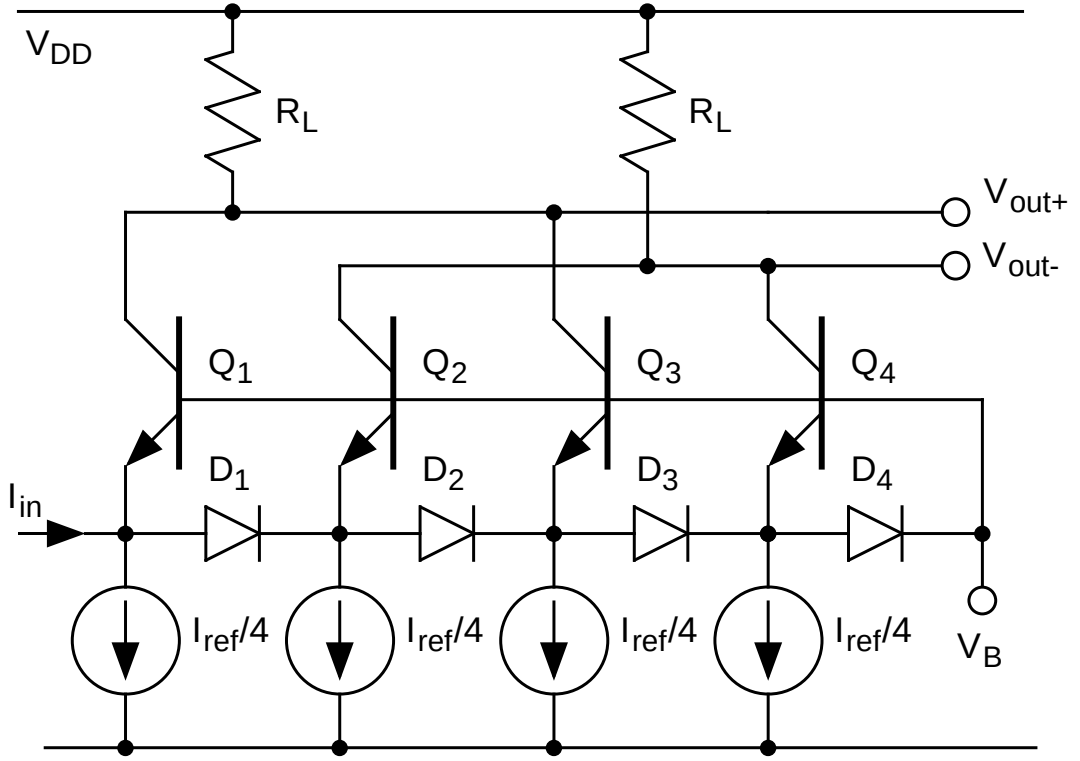
$$V_{out} = V_{in} - \frac{j}{k}V_{ref} \quad \text{for } \frac{j}{k}V_{ref} < V_{in} \le \frac{j+1}{k}V_{ref}, \text{ j even}$$

$$V_{out} = \frac{j+1}{k}V_{ref} - V_{in} \quad \text{for } \frac{j}{k}V_{ref} < V_{in} \le \frac{j+1}{k}V_{ref}, \text{ j odd}$$



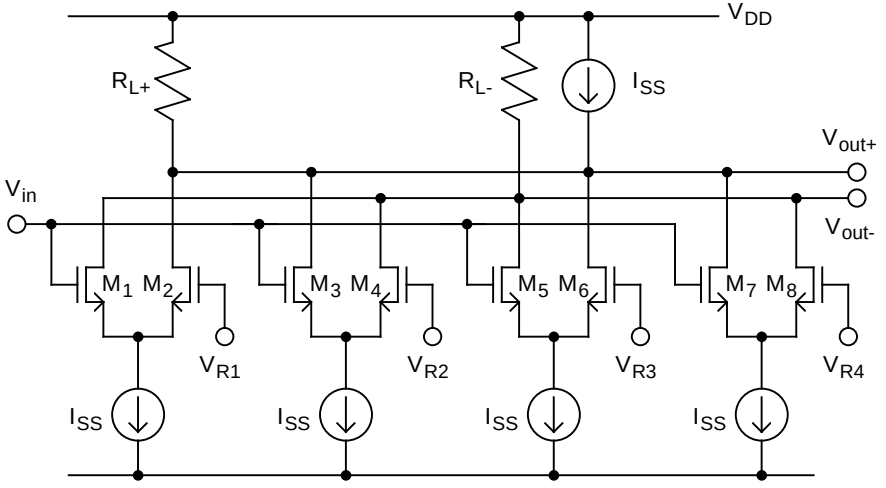
# BIPOLAR FOLDING A/D CONVERTERS

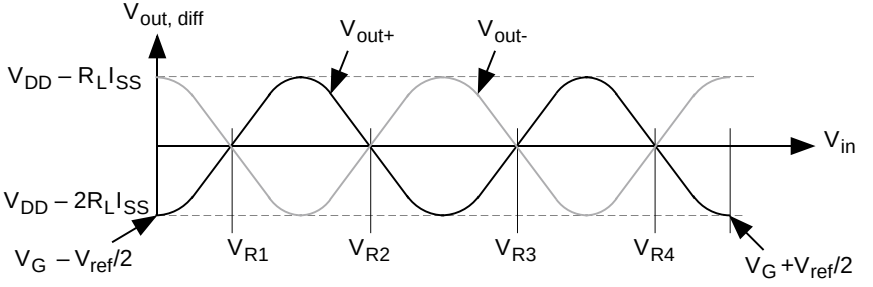
$$I_{in} < \frac{I_{ref}}{4} \begin{cases} V_{out+} = V_{DD} - R_L I_{ref}/2 + R_L I_{in} \\ V_{out-} = V_{DD} - R_L I_{ref}/2 \end{cases} \qquad I_{in} < \frac{I_{ref}}{2} \begin{cases} V_{out+} = V_{DD} - R_L I_{ref}/4 \\ V_{out-} = V_{DD} - R_L I_{ref}/2 + R_L I_{in} \end{cases}$$



# CMOS FOLDING A/D CONVERTERS

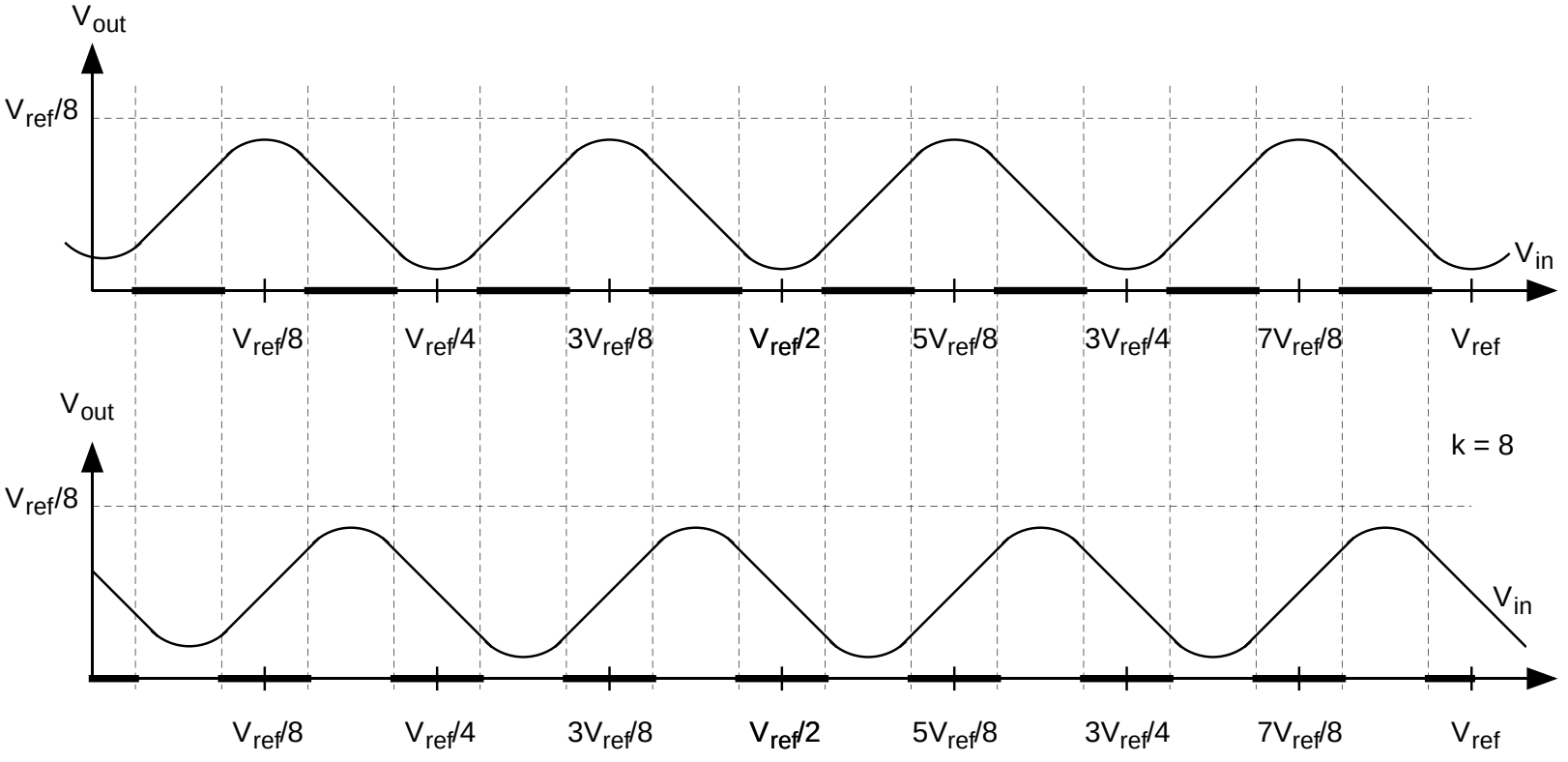
- The linear region of the input-output transfer characteristic depends on the overdrive voltage of the differential pairs
  - ☹ Smaller overdrive ➜ Steeper slope and wider corners
  - ☹ Larger overdrive ➜ Full swing not achievable
- The gain depends on the $g_m R_L$ product



# DOUBLE-FOLDING A/D CONVERTERS

- Rounding in the transitions between segments ➜ Significant error in a wide range near the segment margins

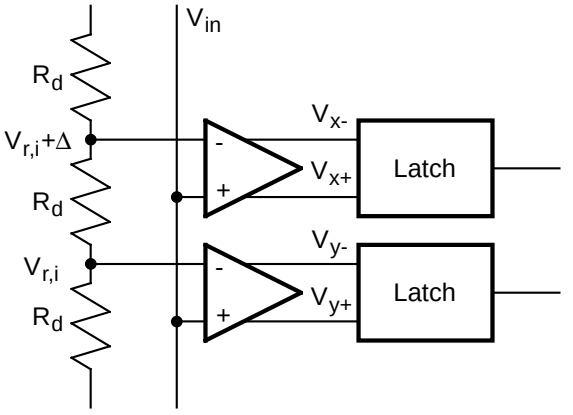


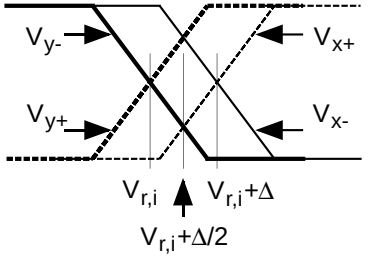
# FOLDING A/D CONVERTERS

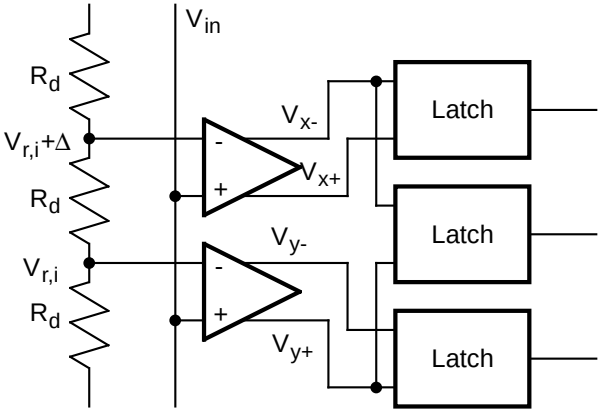
- The current gain β of bipolar transistors, the matching between MOS transistors, the inaccuracy of current sources and the mismatch of load resistances influence the precision
- Typical values of β and typical matching performances in integrated technology lead to an error of the range of 0.1%
  - ➥ Maximum resolution is 10 bit
- Speed of bipolar implementations ➜ More than 100 MHz
- Speed of CMOS implementations ➜ Depends on the feature size of the technology

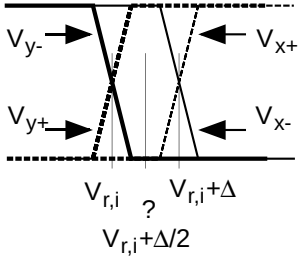
# INTERPOLATING A/D CONVERTERS

- Interpolation ➜ Reduced complexity
- The interpolation technique can be applied in the situations where two analog signals can be used to determine the same digital code
- The interpolation technique allows us to extract one or more additional codes

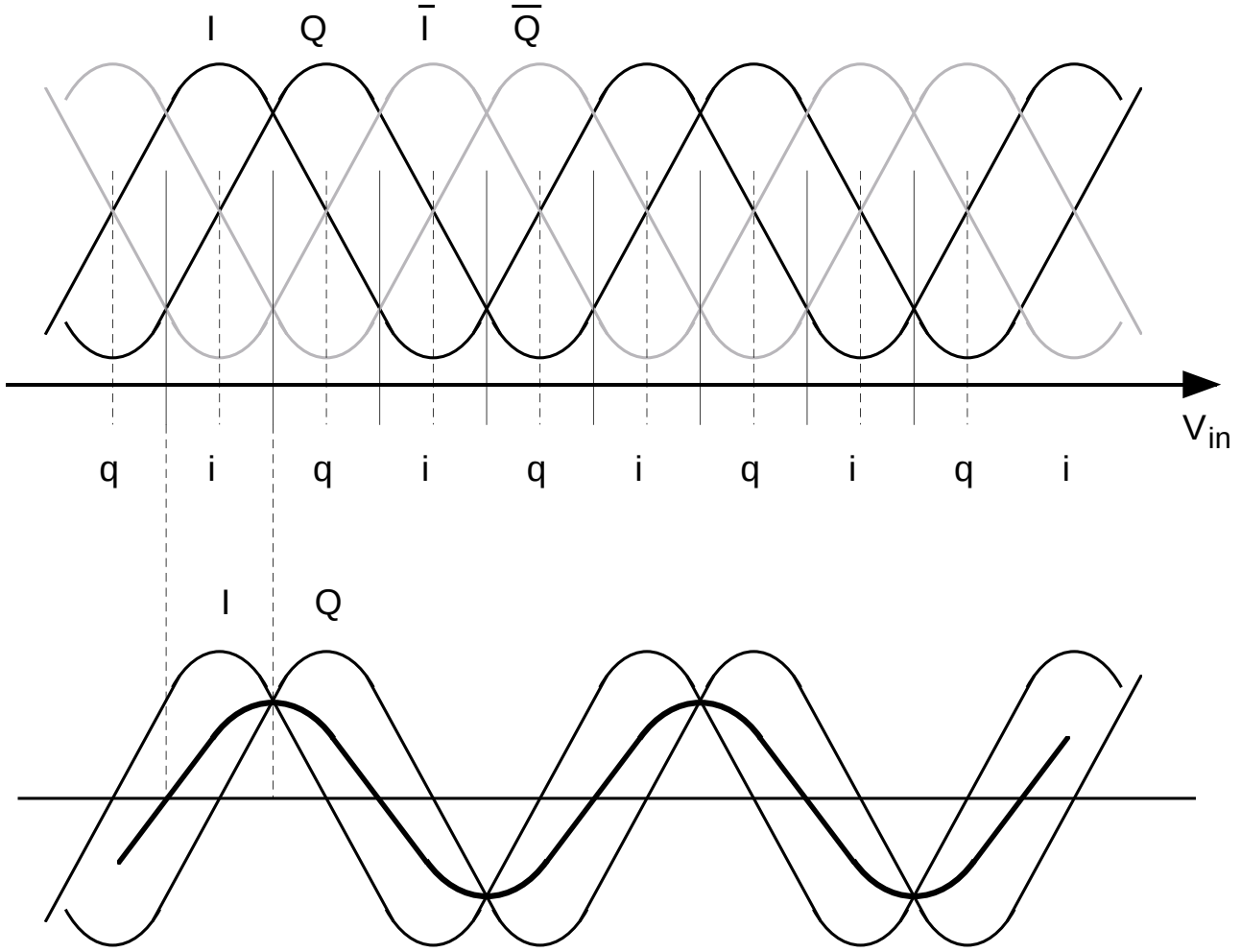


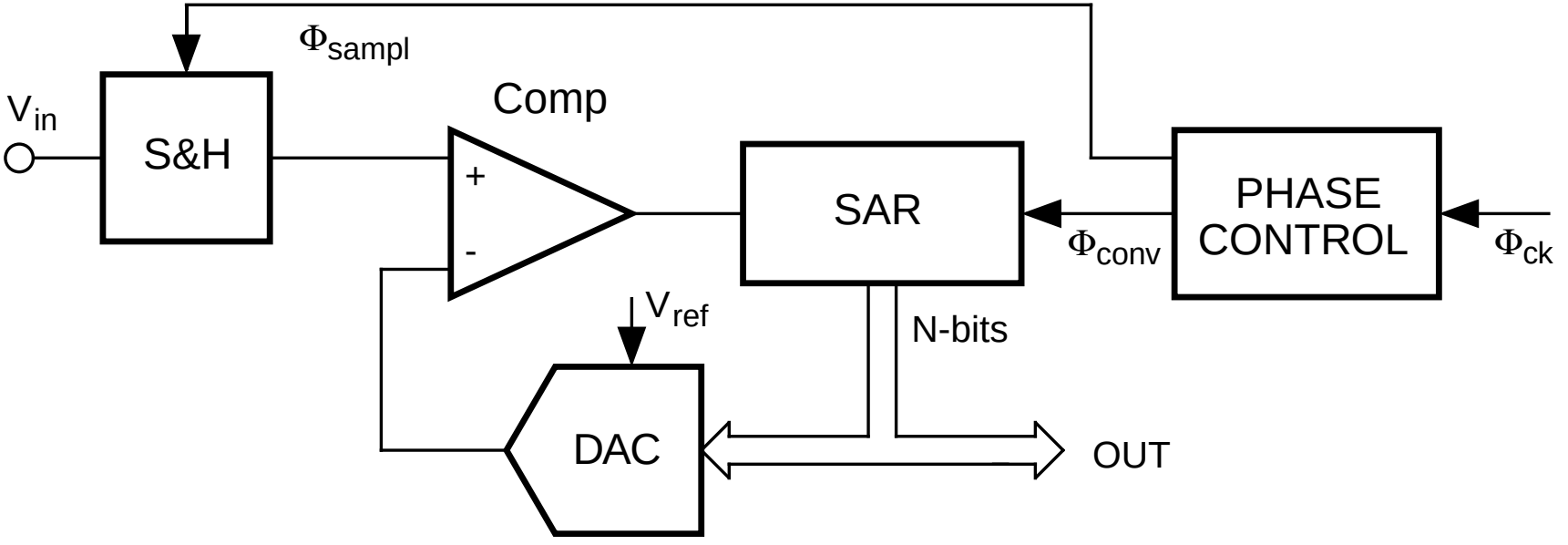



# FOLDING-INTERPOLATING A/D CONVERTERS



# SUCCESSIVE APPROXIMATION A/D CONVERTERS

- Successive approximation A/D converters ➜ Optimal solution for medium speed and moderate accuracy (10-12 bit)
- Conversion time for N bits of resolution ➜ N + 1 clock cycles (one clock cycle is required for sampling the input signal)



# SUCCESSIVE APPROXIMATION A/D CONVERTERS

- The Sample and Hold (S&H) block samples the input signal at the beginning of each conversion cycle
- A Successive Approximation Register (SAR) controls the Digital-to-Analog Converter (DAC) which generates the proper sequence of approximations
- The Comparator (Comp) compares the approximations generated by the DAC with the output of the S&H and determines one bit of the digital output in each clock period
- The logic used is based on the binary search starting from the Most Significant Bit (MSB)

# SUCCESSIVE APPROXIMATION A/D CONVERTERS

- Principle of operation ➜ The digital representation B $(b_{N-1}, b_{N-2}, \ldots, b_0)$ of an analog signal $V_{in}$ is

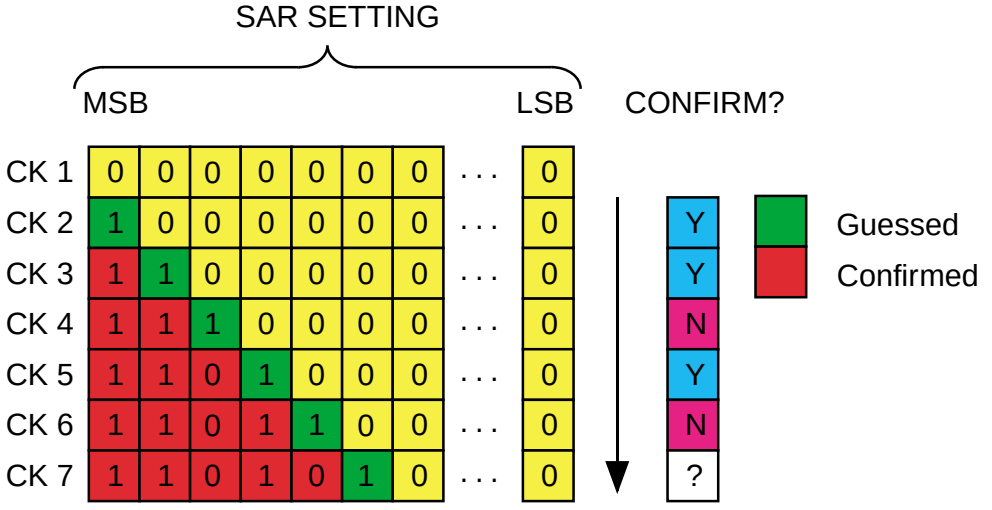
$$V_{in} = \frac{V_{ref}}{2} b_{N-1} + \frac{V_{ref}}{2^2} b_{N-2} + \ldots + \frac{V_{ref}}{2^N} b_0 + \frac{V_{ref}}{2^{N+1}} + \varepsilon_Q$$

  - ➥ $V_{ref} / 2^{N+1}$ ➜ 1/2 LSB shift of the transfer characteristic
  - ➥ $\varepsilon_Q$ ➜ Quantization error

- The MSB $b_{N-1}$ is determined with a comparison between $V_{in}$ and $V_{ref} / 2$
- The next bit $b_{N-2}$ is determined with a comparison between $V_{in}$ and $b_{N-1}\, V_{ref} / 2 + V_{ref} / 4$

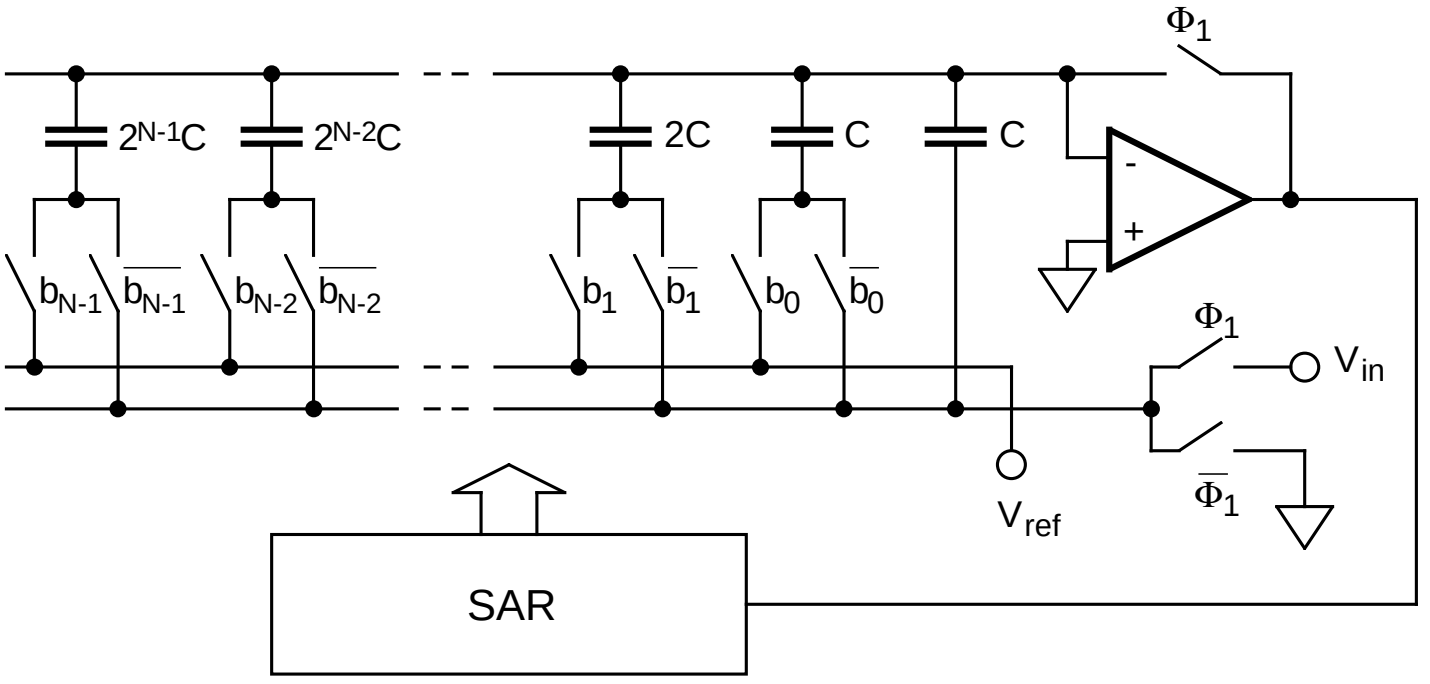
# SUCCESSIVE APPROXIMATION REGISTER

- Successive approximation register (SAR) ➜ Control of the DAC
  - Sampling of the input ➜ CK 1
  - The conversion cycle starts at CK 2 ➜ MSB = 1, LSBs = 0
  - The decision of the comparator successively determines the value of the bits



# SUCCESSIVE APPROXIMATION A/D CONVERTERS

- Charge redistribution A/D converter
  - ☺ The comparator operates referred to ground instead of processing the output of the DAC and the sampled input



# SUCCESSIVE APPROXIMATION A/D CONVERTERS

- During the first clock period the circuit samples the input
- The total charge stored on the capacitive array is

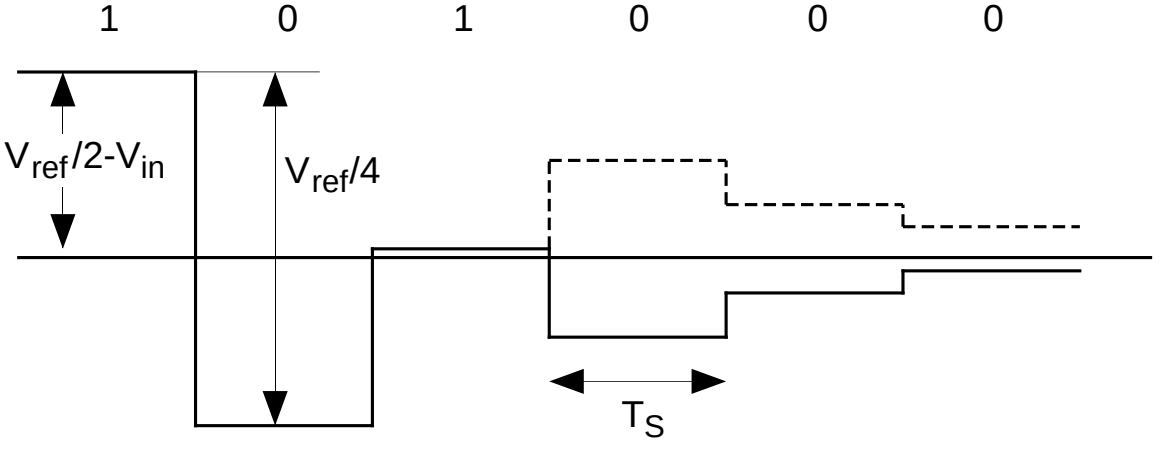
$$Q_{tot} = 2^N C(V_{in} - V_{os})$$

- Sampling period ➜ The operational amplifier is buffer connected
- Conversion cycle ➜ The operational amplifier is used in open loop as a comparator
- After the determination of the MSB, the voltage at the inverting input of the comparator becomes

$$V_x = \frac{2^{N-1}C}{C_{tot}} V_{ref} - (V_{in} - V_{os}) = \frac{1}{2} V_{ref} - V_{in} + V_{os}$$

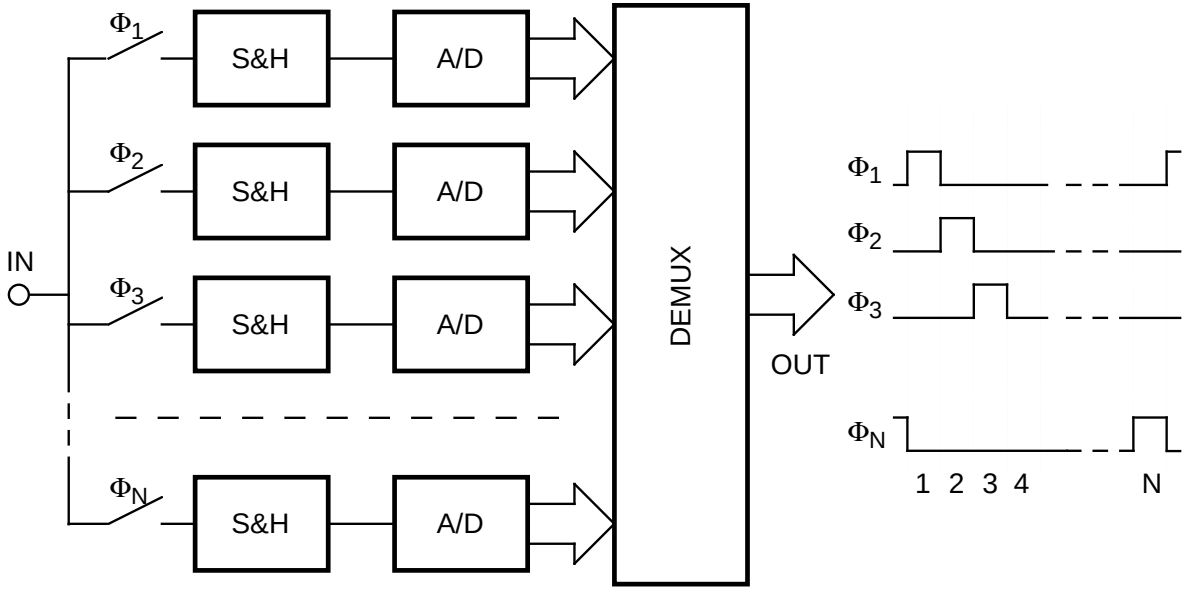
# SUCCESSIVE APPROXIMATION A/D CONVERTERS

- Charge on capacitor $2^{N-1}C$ ➜ $Q_{C_{N-1}} = 2^{N-1}C\left(\frac{V_{ref}}{2} + V_{in} - V_{os}\right)$
- The total charge on the top plate is unchanged ➜ The remaining charge is distributed in the rest of the capacitive array
- Drawback ➜ Overdrive recovery of the comparator



# INTERLEAVED A/D CONVERTERS

- The conversion speed increases by using N A/D converters interleaved
- The analog multiplexer placed at the input of the circuit connects sequentially the input terminal to one of the conversion channels



# INTERLEAVED A/D CONVERTERS

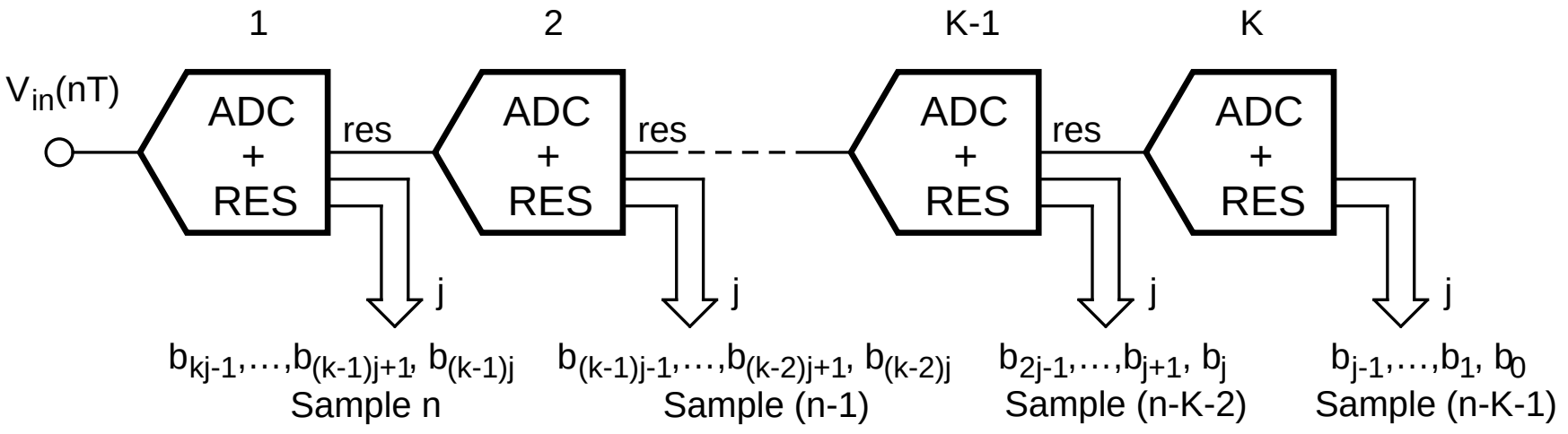
- The sampling rate of the input is 1 / T while the time allowed for the conversion in each channel (including the sampling) is N T
- The converters work with at N times lower sampling rate than the system
- The digital multiplexer at the output receives the digital results from the slow converters and provides the interleaved output at the full data rate
- The interleaved architecture allows slow converters to be used but requires full speed operation in the Sample and Hold (S&H)
- The input signal must be sampled with an error smaller than 1 / 2 LSB during the sampling period T

# INTERLEAVED A/D CONVERTERS

- Limitations of interleaved A/D converters
  - ☹ If one conversion channel is affected by an error, every N clock cycles the output changes ➜ Spur signal at frequency $f_S$ / N
  - ☹ Often, the sampling frequency ($f_S$ = 1 / T) is slightly higher than the Nyquist limit ➜ The spur signal falls in the signal band causing a degradation of the SNR
  - ☹ The non-idealities that are often responsible of the above described distortion are gain error and offset
- Solution ➜ Use analog or digital calibration on-line or off-line, eventually self-calibration, to correct the errors

# PIPELINE A/D CONVERTERS

- Pipeline A/D converter ➜ Cascade of stages operating in parallel each producing one or more bits
- Bits relative to successive input samples are determined during the same clock cycle
- The sampling rate increases at the expense of a system latency

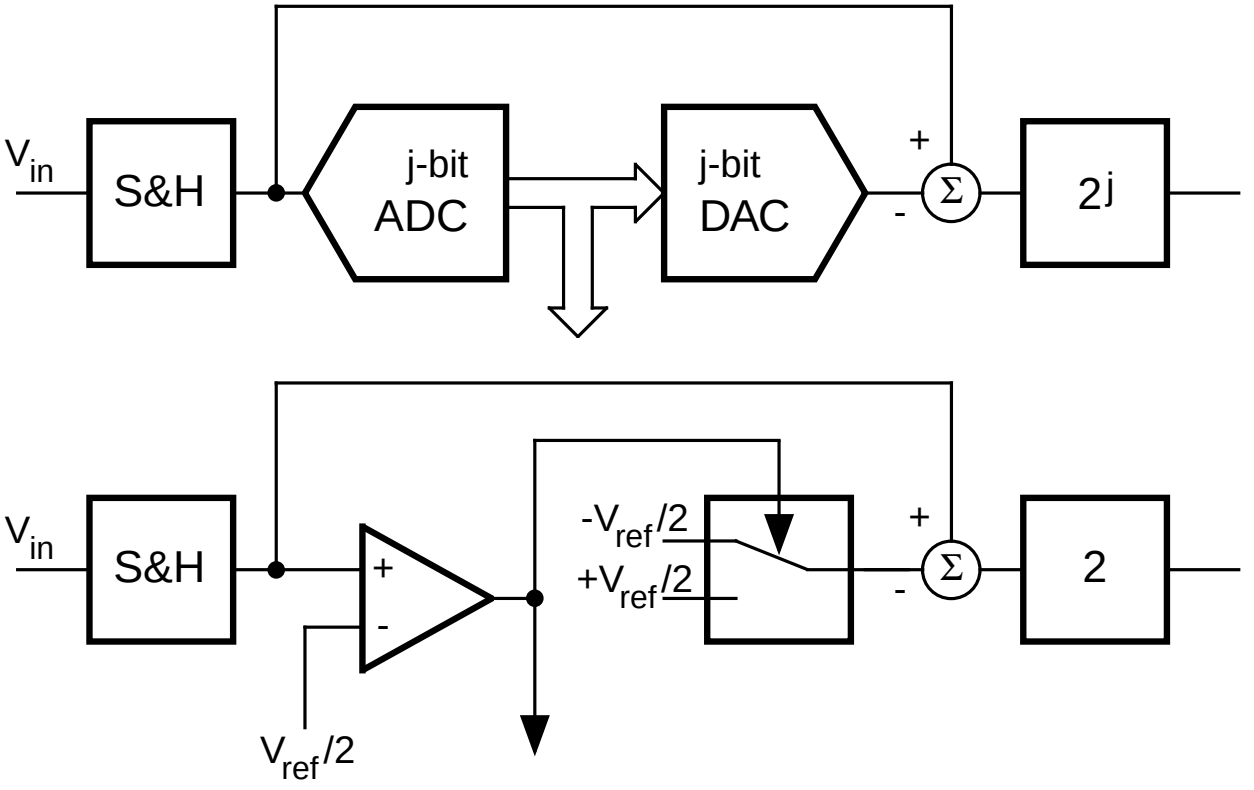



# PIPELINE A/D CONVERTERS

- The signal processing in the analog path must preserve the information content of the residual bits
- The circuit complexity and the power consumption in a pipeline stage are significantly lower than in a complete data converter
- The pipeline architecture achieves a better trade-off between speed, area and power consumption with respect to the interleaved architecture
- The total number of stages K required to obtain a given resolution decreases as the number of bits of each stage increases, but the analog processing required for each stage also increases at the expense of speed and the power consumption ➜ Trade-off

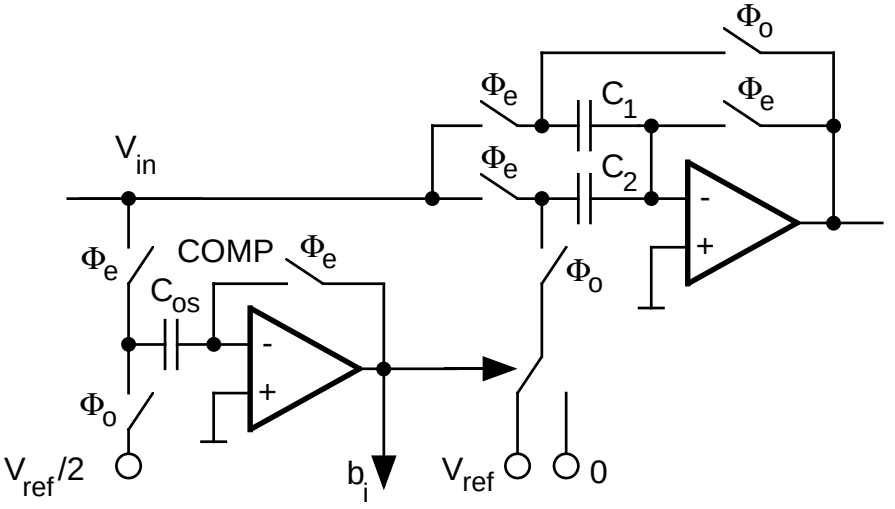
# PIPELINE A/D CONVERTERS

- Typically few bits per stage are used ➜ CMOS switched capacitor implementation of a one bit per stage pipeline A/D converter



# PIPELINE A/D CONVERTERS

- During the even clock phase $\Phi_e$ the circuit samples the input voltage on two equal capacitors $C_1$ and $C_2$ and the comparator performs the auto-zero by storing the offset on capacitor $C_{os}$
- During the odd clock phase $\Phi_o$ capacitor $C_1$ is connected in feedback ➜ $C_1$ receives the charge delivered by $C_2$



# PIPELINE A/D CONVERTERS

- The charge transfer between $C_1$ and $C_2$ is offset insensitive since they have been pre-charged to the offset of the amplifier
- The left plate of the auto-zero capacitor switches toward the threshold voltage $V_{ref} / 2$ ➜ The amplifier, operated in open-loop condition, provides the bit value
- The 1-bit DAC charges $C_2$ with $V_{ref}$ or 0, depending on the bit value ➜ The analog output is given by

$$V_{out} = V_{in}\left(1 + \frac{C_2}{C_1}\right) - b_j V_{ref}\frac{C_2}{C_1}$$

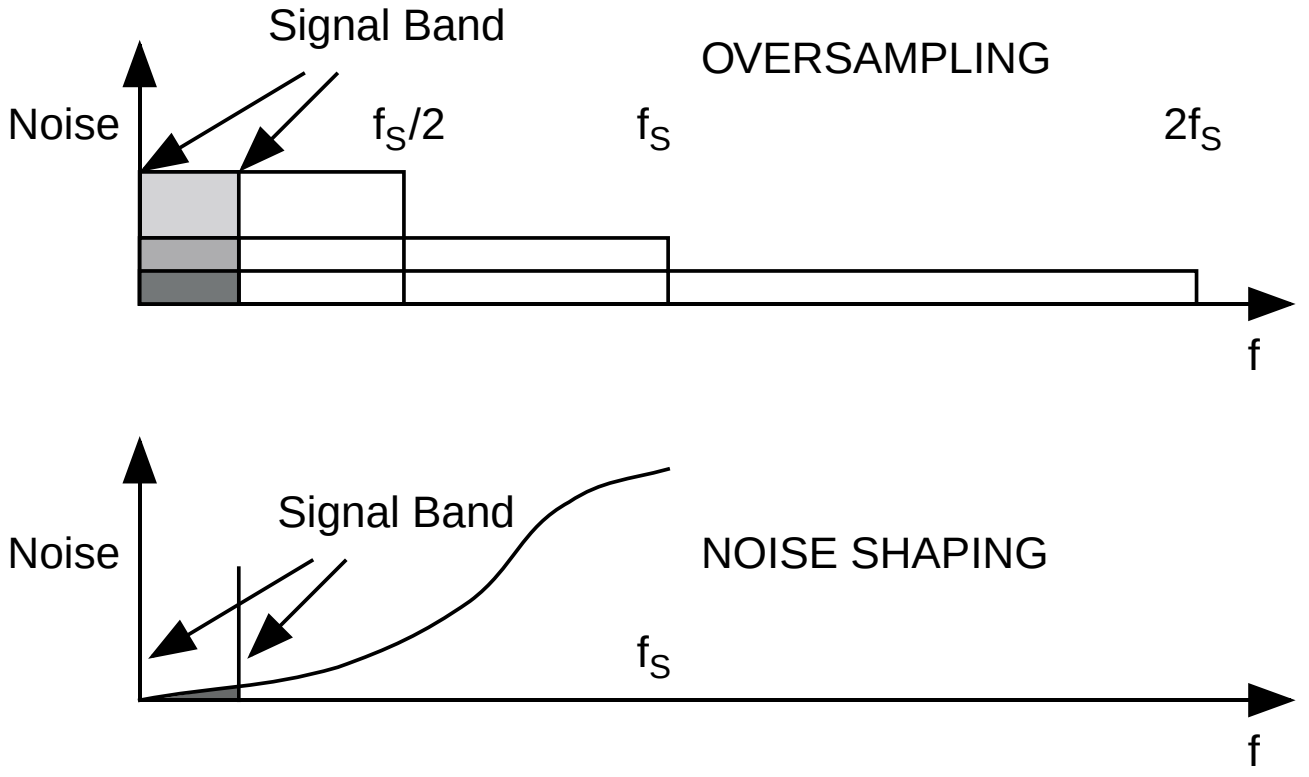
- Capacitors $C_1$ and $C_2$ are equal ➜ The circuit multiplies the input by two

# OVERSAMPLED A/D CONVERTERS

- The effective number of bits of an A/D converter can be increased by using oversampling techniques
- If the sampling frequency is higher than the Nyquist limit only a fraction of the quantization noise power falls in the signal band
- A digital filter which rejects the out-of-band noise is required to increase the effective number of bits
- Modern technologies allow higher and higher frequency of operation either in digital and in analog sections ➜ For signals with a relatively small band it is possible to trade speed with resolution
- Oversampling ratio ➜ OSR

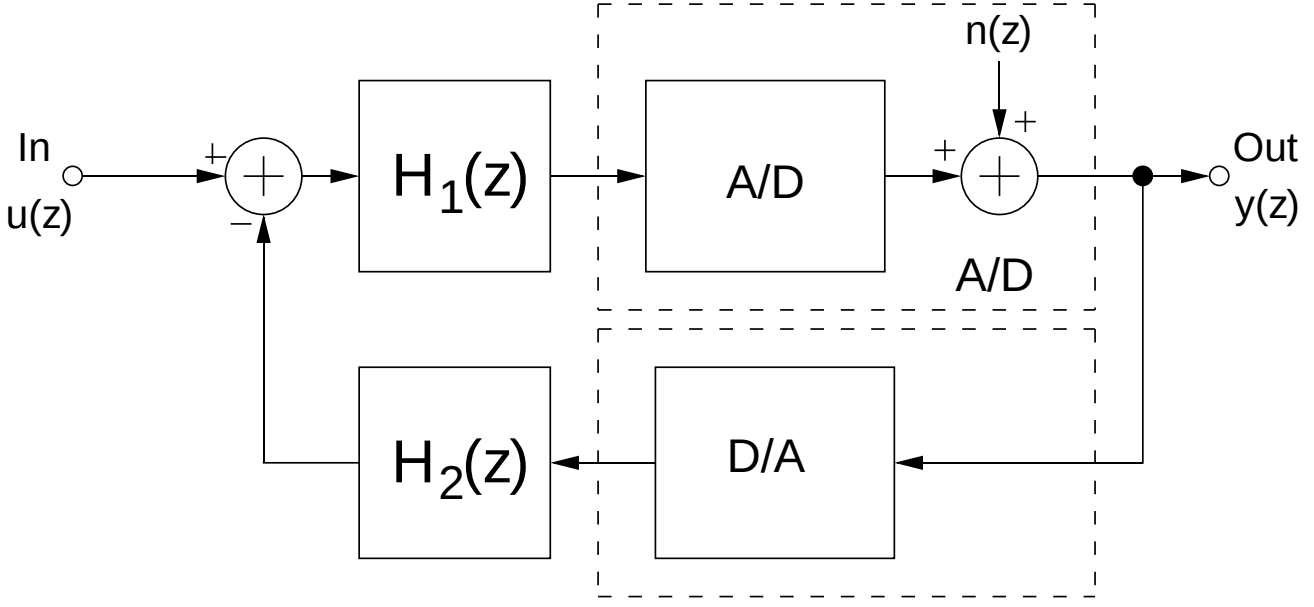
# SIGMA-DELTA MODULATORS

- Noise shaping ➜ Reduce the amount of quantization noise in the signal band, thus increasing the signal-to-noise ratio



# NOISE SHAPING

- Quantizer included in the feedback loop
  - Two inputs (signal and quantization noise) and one output
  - Different transfer functions for the signal and the quantization noise



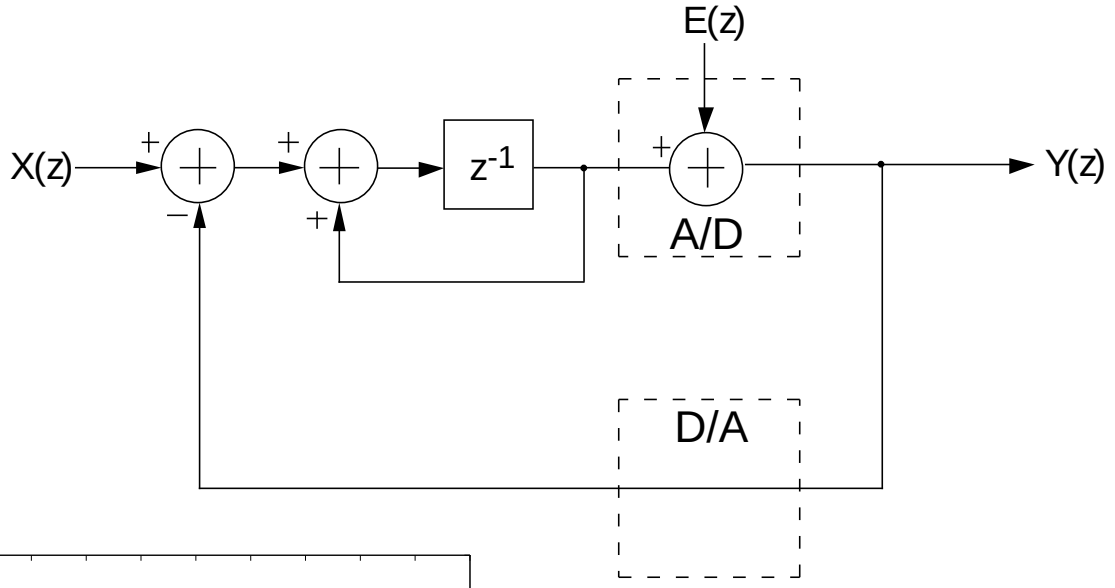
# Signal and Noise Transfer Functions

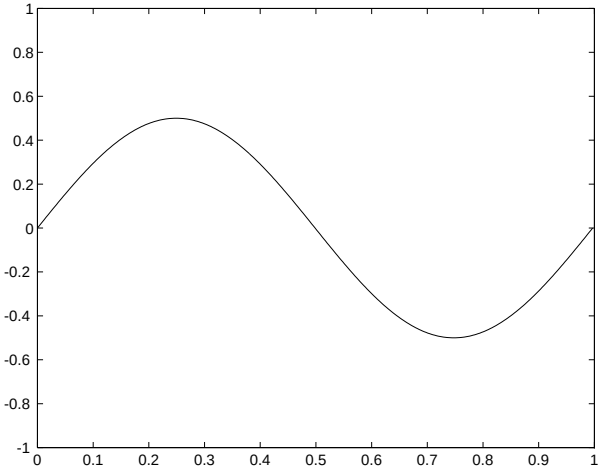
- $y(z) = \frac{H_1(z)}{1 + H_1(z)H_2(z)}u(z) + \frac{1}{1 + H_1(z)H_2(z)}n(z)$
- Signal transfer function ➜ $STF(z) = \frac{H_1(z)}{1 + H_1(z)H_2(z)}$
- Noise transfer function ➜ $NTF(z) = \frac{1}{1 + H_1(z)H_2(z)}$
- Typical architecture
  - ➥ $STF(z) = 1$
  - ➥ $NTF(z) = (1 - z^{-1})^L$, L ➜ Order of the sigma-delta modulator

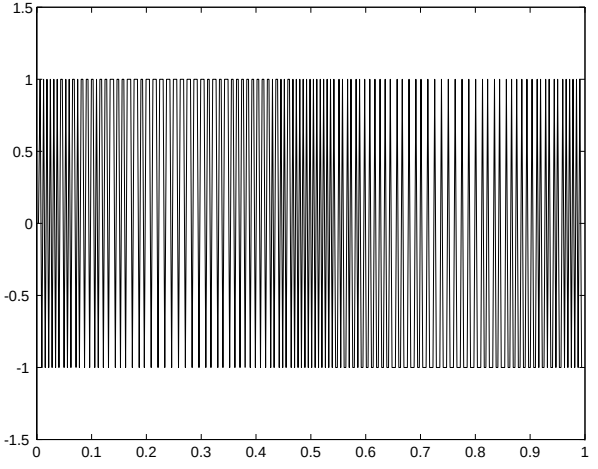
# First Order Sigma-Delta Modulator

- Single bit A/D and D/A converters
- $H_1(z)$ ➜ Integrator

  $H_1(z) = z^{-1}/(1 - z^{-1})$
- $H_2(z)$ ➜ 1




$$NTF(z) = (1 - z^{-1})$$

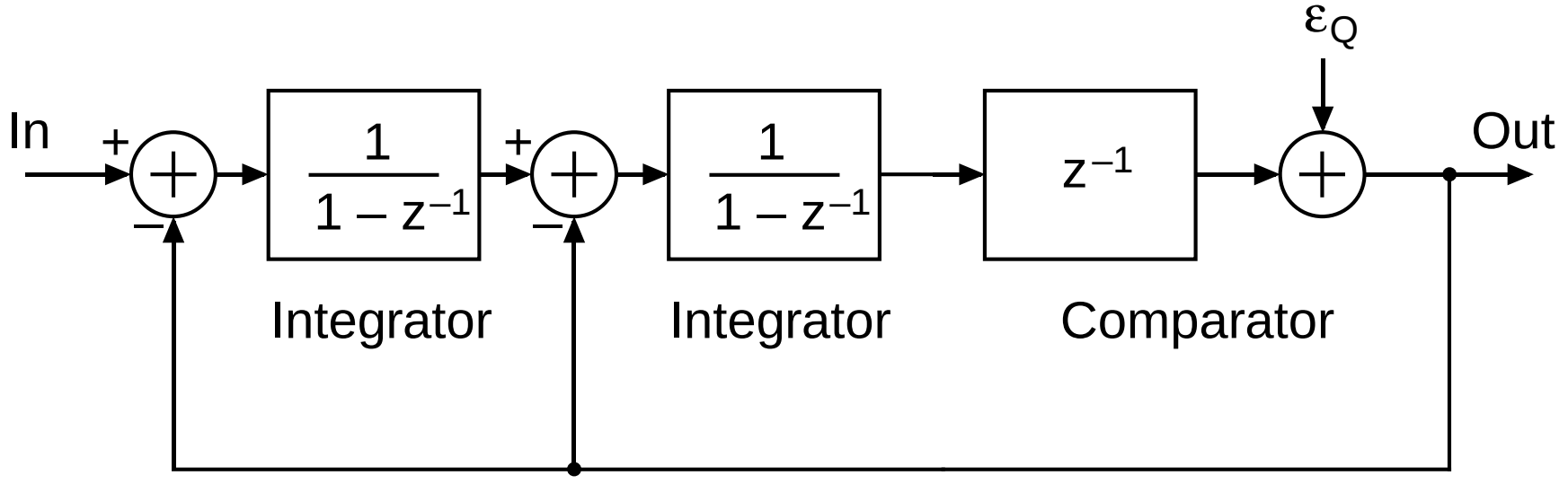
# First Order Sigma-Delta Modulator

- $NTF(z) = (1 - z^{-1}) = (1 - e^{-j\omega T_S}) = e^{-j\omega T_S/2} 2j\sin(\omega T_S/2)$
- $P_{noise} = \int_0^{f_B} \frac{P_Q(f)}{1/(2T_S)} NTF(f)^2 df \approx P_Q \frac{\pi^2}{3} (2f_B T_S)^3 = P_Q \frac{\pi^2}{3} OSR^{-3}$
- For an input sinewave the RMS signal power is $\Delta^2/8$ and the SNR becomes

$$SNR = 10\log \frac{\frac{OSR^3 \Delta^2}{8}}{\left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^2}{3}\right)} = -3.14 + 9.03\log_2(OSR) = 6.02N$$

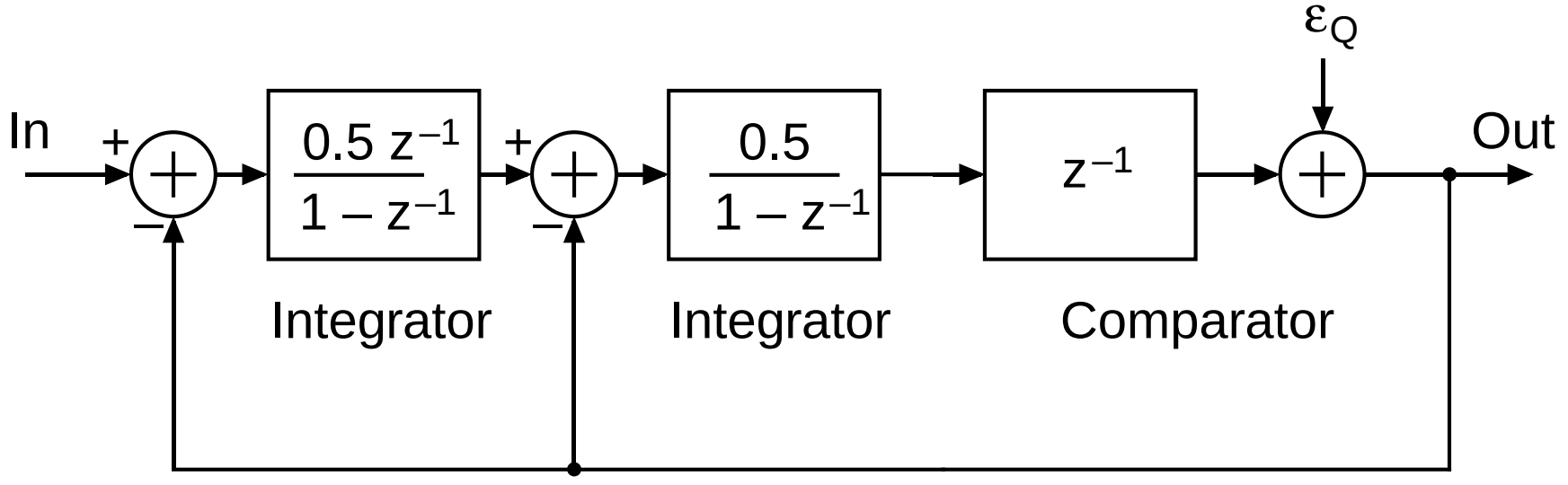
# SECOND ORDER SIGMA-DELTA MODULATOR

- Two integrators around the feedback loop
- Signal transfer function ➜ $STF(z) = z^{-1}$
- Noise transfer function ➜ $NTF(z) = (1 - z^{-1})^2$



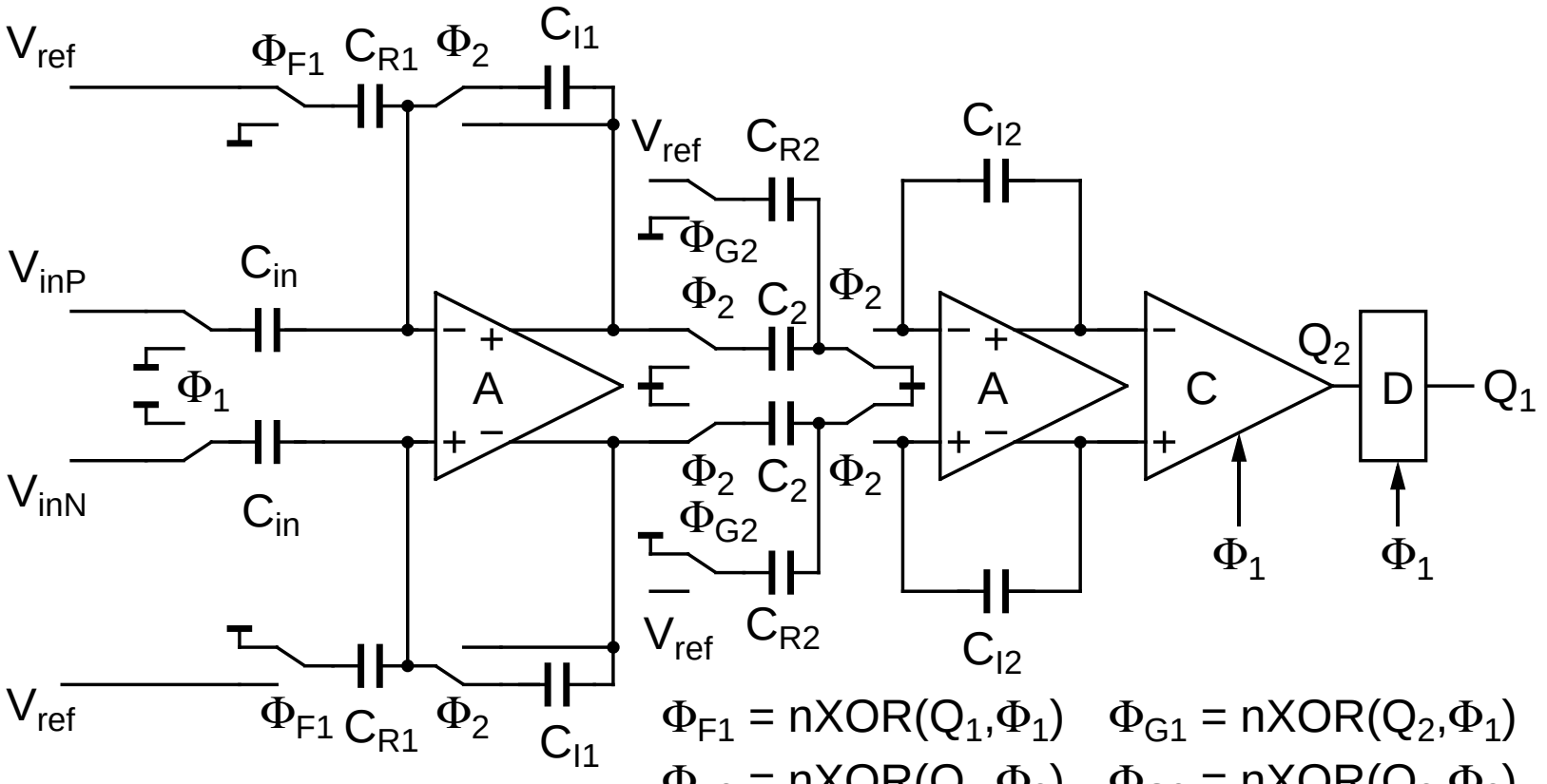
# SECOND ORDER SIGMA-DELTA MODULATOR

- Two integrators around the feedback loop
- Signal transfer function ➜ $STF(z) = z^{-2}$
- Noise transfer function ➜ $NTF(z) = (1 - z^{-1})^2$



# SECOND ORDER SIGMA-DELTA MODULATOR

- Switched-capacitor implementation

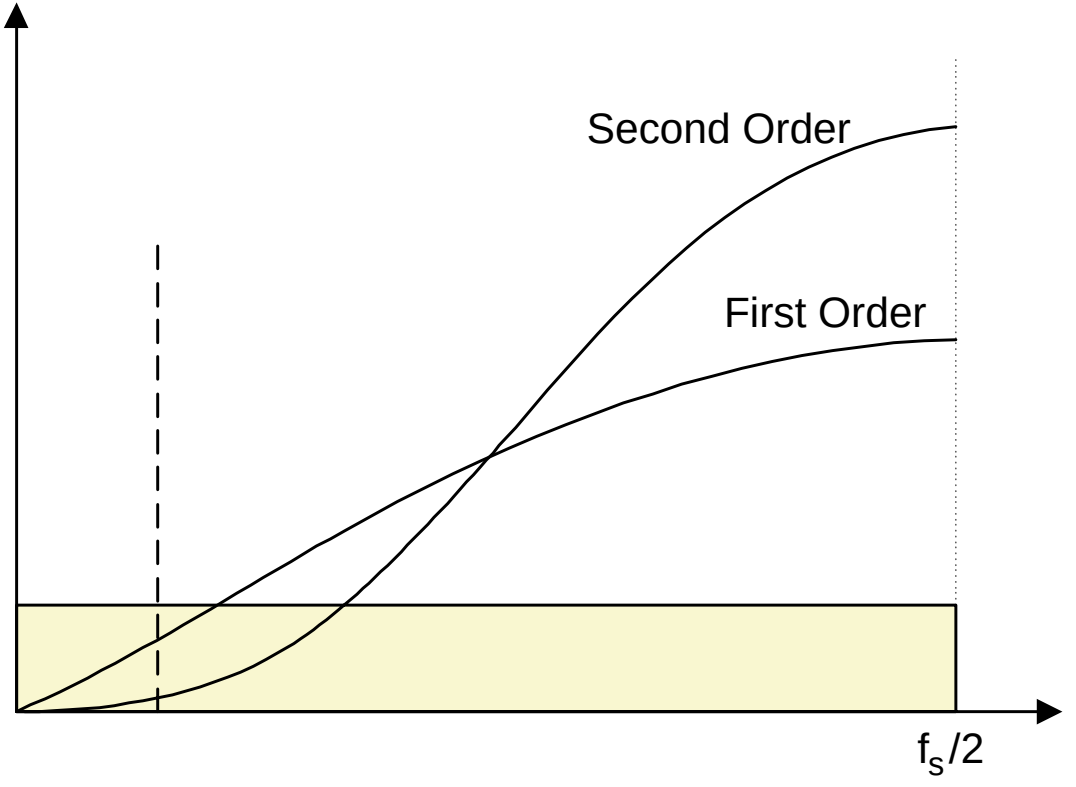



$\Phi_{F1} = nXOR(Q_1,\Phi_1)$ $\Phi_{G1} = nXOR(Q_2,\Phi_1)$

$\Phi_{F2} = nXOR(Q_1,\Phi_2)$ $\Phi_{G2} = nXOR(Q_2,\Phi_2)$

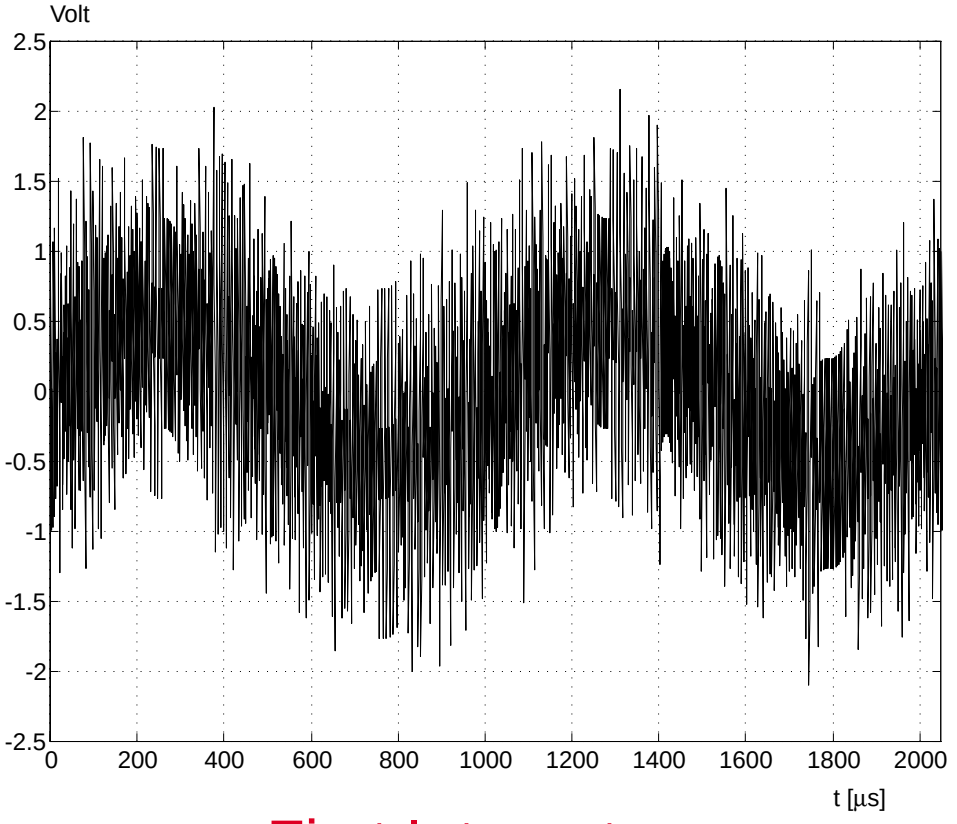
# NOISE SHAPING

- The in-band noise is reduced, while the out-of-band noise is enhanced

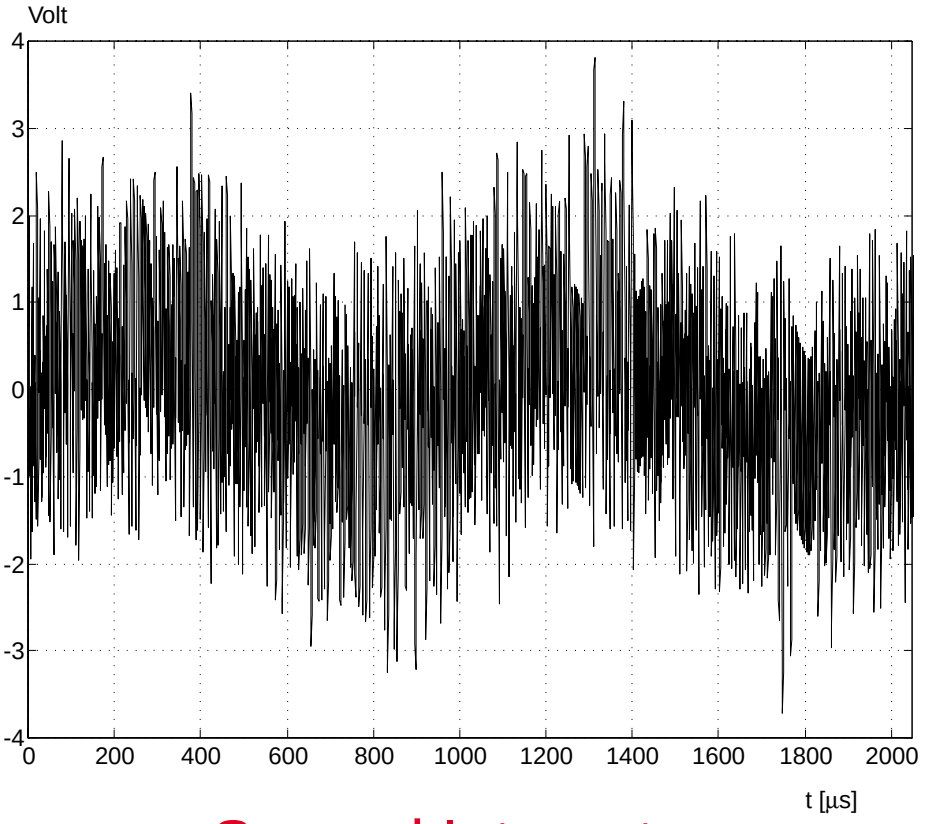



# INTEGRATOR OUTPUT SWING

## Second Order Sigma-Delta Modulator

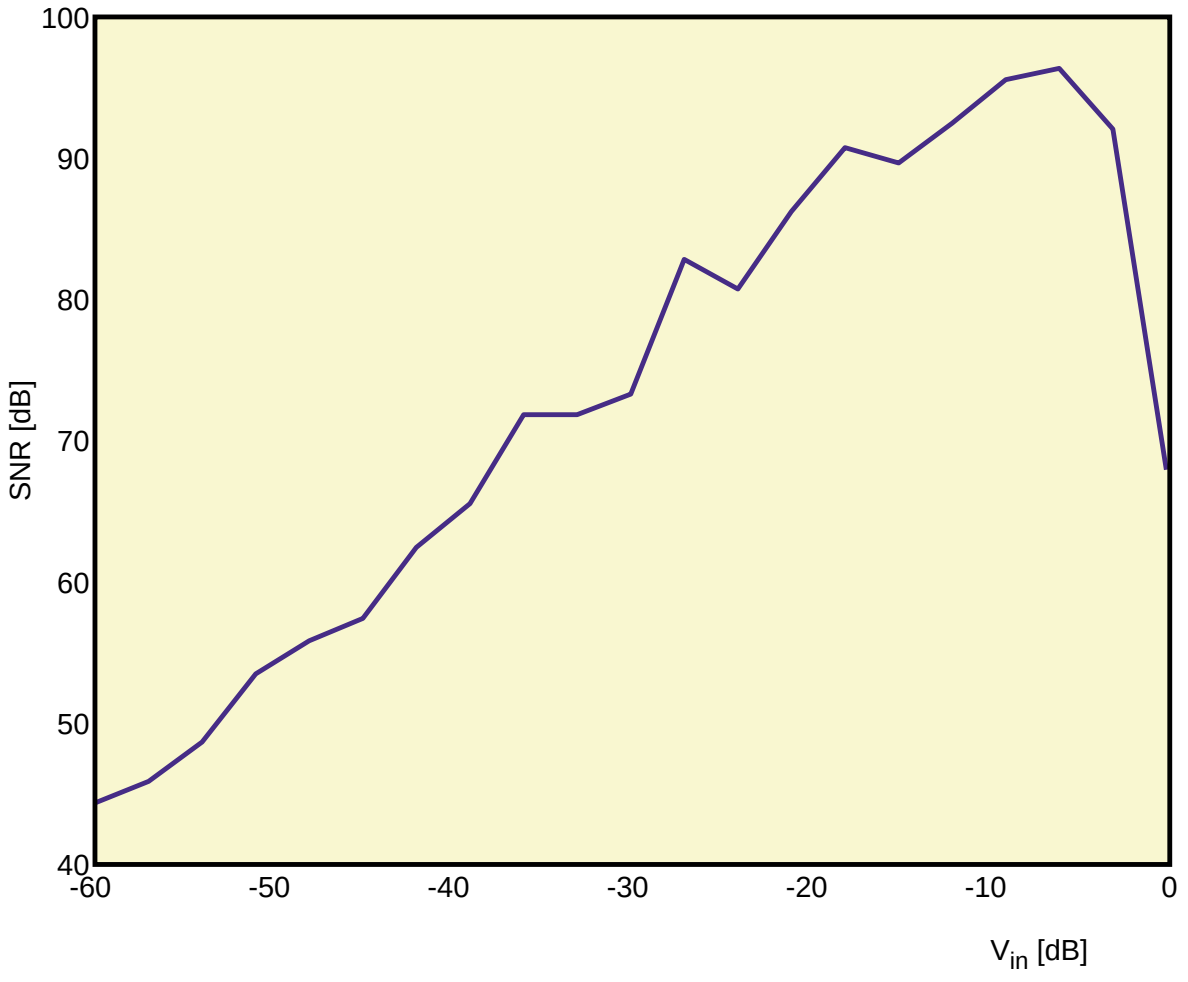



First Integrator




Second Integrator

# SIGNAL-TO-NOISE RATIO VS INPUT AMPLITUDE




Second Order Sigma-Delta Modulator

# QUANTIZATION NOISE POWER

- In-band noise power for an Lth-order sigma-delta modulator

$$P_Q = \frac{\Delta^2 \pi^{2L}}{2^{2N}(2L+1)3OSR^{(2L+1)}}$$

$$SNR = \frac{2^{2N}(2L+1)3OSR^{(2L+1)}}{2\pi^{2L}}$$

  - ➥ $\Delta$ ➜ Full scale voltage, N ➜ Number of bits of the quantizer, L ➜ Order of modulator, OSR ➜ Oversampling ratio, Signal amplitude ➜ $\Delta^2/8$

- The in-band quantization noise decreases 3 (2 L + 1) dB per octave of oversampling and 6 dB per additional bit of quantizer resolution

# SIGMA-DELTA MODULATOR NON-IDEALITIES

- Clock Jitter
- Integrator thermal and k T / C noise
- Operational amplifier finite gain
- Operational amplifier finite bandwidth
- Operational amplifier finite slew-rate
- Continuous-time vs switched-capacitor and single-bit vs multi-bit

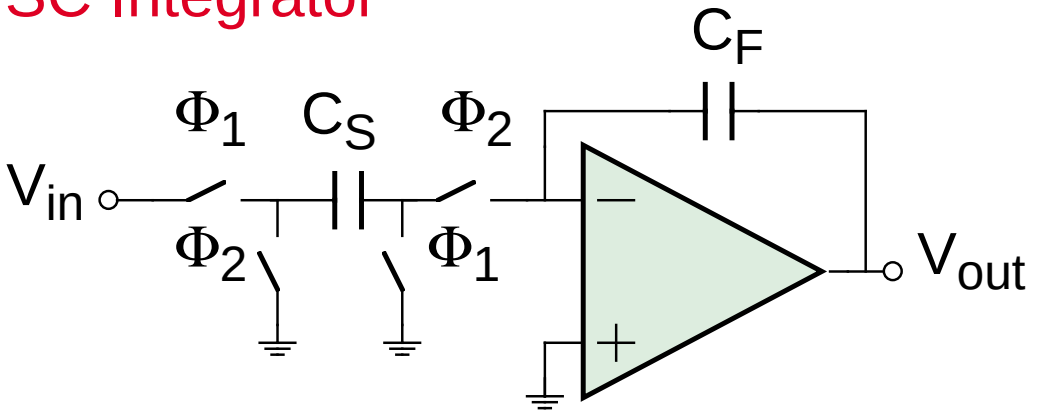
# CLOCK JITTER

- SC ΣΔ modulator ➜ Sampled data system
  - The clock jitter effect is restricted to the input signal sampling
  - Sampling clock jitter ➜ Non-uniform sampling
  - The error introduced is a function of both the input signal and the statistical properties of the jitter
- Error due to a clock jitter $\delta$ when sampling a sinusoidal signal x(t) with amplitude A and frequency $f_{in}$
  - $x(t+\delta) - x(t) \approx 2\pi f_{in}\delta A\cos(2\pi f_{in}t) = \delta\frac{d}{dt}x(t)$
  - Gaussian clock jitter with standard deviation $\Delta\tau$ ➜ White noise with power $P_j = (2\pi f_{in}\Delta\tau A)^2/2$, integrated from 0 to $f_S / 2$

# SWITCHED-CAPACITOR INTEGRATOR NOISE

- Noise sources in a SC ΣΔ modulator
  - ➥ Thermal noise in the sampling switches of the integrators
  - ➥ Intrinsic noise of the operational amplifiers
  - ☺ Large DC gain of the first integrator ➜ Noise performance determined by the input stage

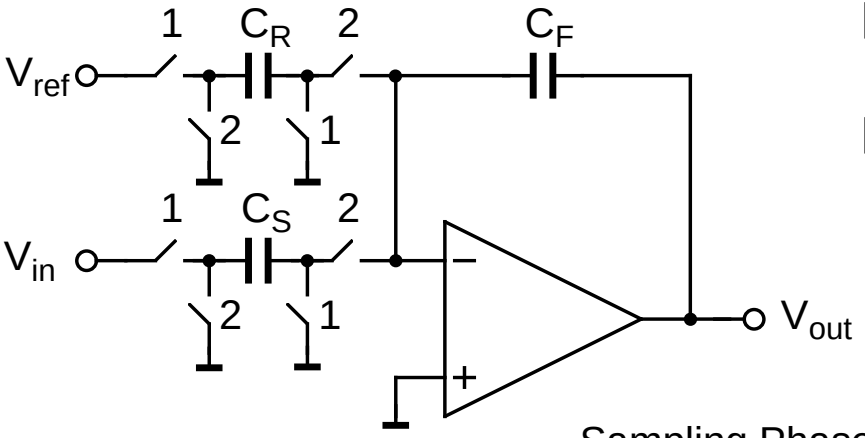
SC Integrator




$$\text{Integrator Gain} \rightarrow \beta = \frac{C_S}{C_F}$$

$$e_T^2 = \int_0^\infty \frac{4kTR_{on}}{1+(2\pi f R_{on} C_S)^2} df = \frac{kT}{C_S}$$

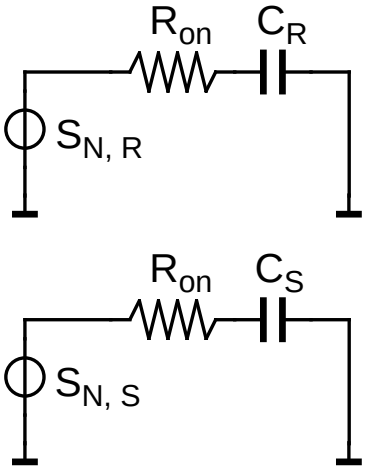
# SWITCHED-CAPACITOR INTEGRATOR NOISE



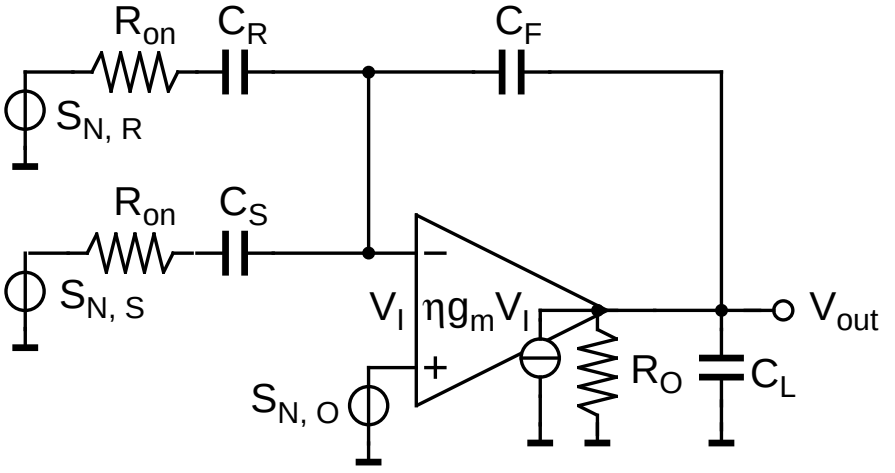

- Main noise source ➜ k T / C
- SC integrator ➜ Time variant network

$$N = \int_0^\infty |NTF|^2 S_N df$$

Sampling Phase (1)




Integration Phase (2)



# SWITCHED-CAPACITOR INTEGRATOR NOISE

- Sampling phase (1)
- Noise Sources ➜ $S_{N,S} = S_{N,R} = 4kTR_{on}$
- $NTF_{S,1} = \dfrac{1}{1 + sC_S R_{on}}$
- $NTF_{R,1} = \dfrac{1}{1 + sC_R R_{on}}$
- Total Power ➜ $N_1 = \dfrac{2kT}{C}$ with $C_S = C_R = C$

# SWITCHED-CAPACITOR INTEGRATOR NOISE

- Integration phase (2)
- Noise Sources → $S_{N,O} = \frac{4kT(1+\gamma)}{3g_m}$, $S_{N,S} = S_{N,R} = 4kTR_{on}$
- $NTF_{S|R,2} = -\frac{1}{2}\frac{\eta g_m + sC_L}{\eta g_m + s(2C_L + 2C + \eta g_m R_{on}) + s^2 C C_L R_{on}}$
- $NTF_{O,2} = \frac{\eta g_m}{\eta g_m + s(2C_L + 2C + \eta g_m R_{on}) + s^2 C C_L R_{on}}$
- Total Power → $N_2 = \frac{2kT(2C + C_L + 2\gamma C + \eta g_m R_{on} C)}{C(2C + 2C_L + \eta g_m R_{on} C)}$

# SWITCHED-CAPACITOR INTEGRATOR NOISE

- Combining all of the noise contribution from both clock phases, we obtain the total thermal noise power

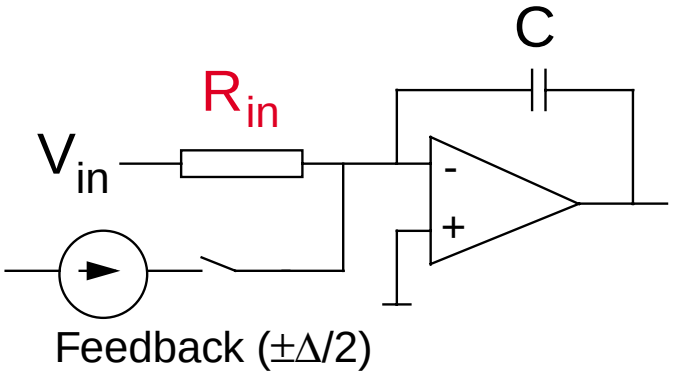
- Total Power ➜ $N_{Th} = \frac{2kT(4C + 3C_L + 2\gamma C + 2\eta g_m R_{on} C)}{C(2C + 2C_L + \eta g_m R_{on} C)}$

- In-Band Power ➜ $P_{Th} = \frac{2kT(4C + 3C_L + 2\gamma C + 2\eta g_m R_{on} C)}{OSRC(2C + 2C_L + \eta g_m R_{on} C)}$

- Typical values of the parameters ➜ $\gamma = 4$, $\eta = 3$, $g_m = 750$ mS and $R_{on} = 1$ kΩ

# CONTINUOUS-TIME INTEGRATOR NOISE

- The thermal noise generator of the input resistance is in series with the input signal ➜ The noise power in the signal band B is $v_n^2 = 4kTR_{in}B$
- Upper limit of $R_{in}$ ➜ $R_{in} < \Delta^2/(4kTB10^{SNR/10})$
- Lower limit of C ➜ $C > T_s(4kTB10^{SNR/10})/\Delta^2$
- The operational amplifier noise is treated as usual in continuous-time circuits



# OPERATIONAL AMPLIFIER FINITE GAIN

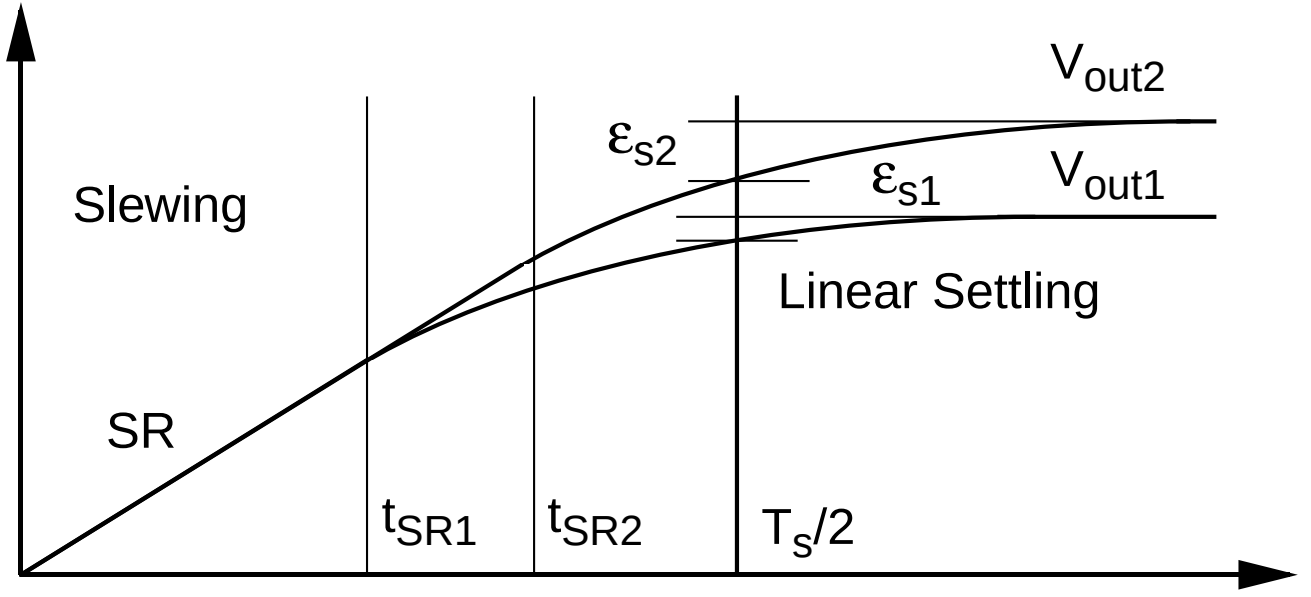
- If the operational amplifier has finite gain $A_o$ the voltage of the non-inverting input is not analog ground but $-V_o / A_o$
- The transfer function of a SC integrator becomes

$$H(z) = \frac{C_S/C_F}{\left(1 + \frac{1}{A_0} + \frac{C_S/C_F}{A_0}\right)z - \left(1 + \frac{1}{A_0}\right)}$$

  - ☹ The integrator shows a gain error (not particularly important) and a phase error
  - ☺ The problem can be alleviated with specific circuit solutions (similar to auto-zero)

# Operational Amplifier Settling

- When the differential input voltage of the operational amplifier exceeds the overdrive voltage of the input stage ➜ Slewing
- The slew-rate SR and the bandwidth GBW = 1 / (2 π τ) of the operational amplifier determine the settling error



# Operational Amplifier Settling

- Operational amplifier settling model
  - $V_{out}(t) \approx V_{out}(0) + SRt_{SR} + \alpha V_{OV}\left(1 - e^{-\frac{(t - t'_{SR})}{\tau}}\right)$ for $t > t_{SR}$
  - Single pole model
  - Time t = 0 corresponds to the beginning of each clock period
  - Parameters $\alpha$ and $t'_{SR}$ model a smooth transition at $t = t_{SR}$
  - The slewing time depends on the input signal
  - The settling region depends on $T_S / 2 - t_{SR}$

$$\varepsilon_S(n) = V_{ov} e^{-\frac{T_S}{2\tau} + \frac{\alpha(V_{in}(n) - V_{ov})}{SR\tau}} \quad \text{where} \quad \alpha = C_S / C_F$$

# OPERATIONAL AMPLIFIER SETTLING

- Spectrum of the settling error

$$P_{\varepsilon_s} df = \frac{(\varepsilon_{max})^2}{12 f_s} df \qquad f \le \frac{f_s}{2}$$

  - The error $\varepsilon_s$ is not correlated with the input signal
  - The error $\varepsilon_s$ is uniformly distributed from 0 to $\varepsilon_{max}$
  - The probability distribution function of $\varepsilon_s$ is uniform

- The settling error power in the signal band is

$$v_s^2 = \frac{V_{ov}^2}{3OSR} e^{-2\left[\frac{1}{2BOSR\tau} - \frac{\alpha\Delta}{SR\tau}\right]}$$

# OPERATIONAL AMPLIFIER SETTLING

- The time allowed for the slewing phase must be a small part (k) of the clock period ➜ $T_S / 2 > k \Delta / SR$ (slew-rate design guideline)
- For a given signal bandwidth B and operational amplifier bandwidth GBW = $1 / (2 \pi \tau)$, the settling error becomes dominant above a given oversampling
- Design guidelines

  ➥ $V_{ov}^2 = \frac{I_D}{K' \frac{W}{L}}$ and $\tau = \frac{C_0}{g_m} = \frac{C_0 V_{ov}}{2 I_D}$

  ☹ The drain current in the input pair must be very large

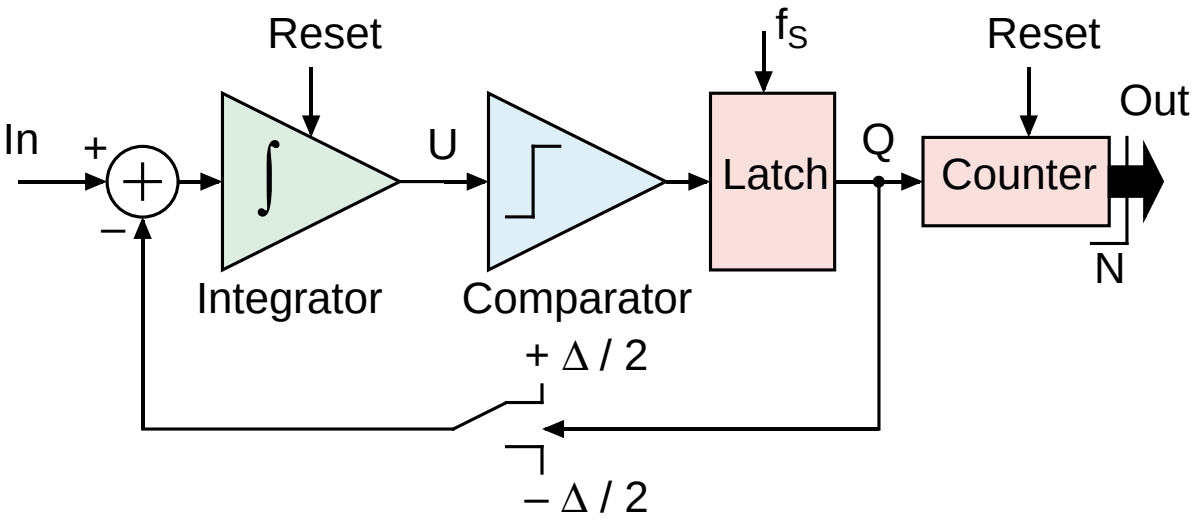
# CONTINUOUS TIME VS SWITCHED CAPACITOR

- Continuous time sigma-delta modulators
  - ☺ The current at the input of the first integrator is continuous-time ➜ The slew-rate requirement is less critical
  - ☺ The input resistance can be external ➜ Very linear and trimmed to the proper value
  - ☹ The clock jitter in the feedback DAC is critical
  - ☹ The time constant of the integrator (R C) varies with the process ➜ The modulator transfer function changes
  - ☹ The feedback DAC requires a very accurate current or charge source, which may increase significantly the power consumption

# SINGLE-BIT VS MULTI-BIT

- Multi-bit sigma-delta modulators
  - ☺ The quantization noise is lower
  - ☺ The quantization noise model is more accurate
  - ☺ The error signal is smaller ➜ Reduced integrator output swing, better stability
  - ☺ Lower modulator order for the same resolution ➜ Simpler decimator
  - ☹ The modulator is more complex
  - ☹ The power consumption increases
  - ☹ The DAC is not inherently linear
  - ☹ Multi-bit output flow

# INCREMENTAL ADC




## Digital Output

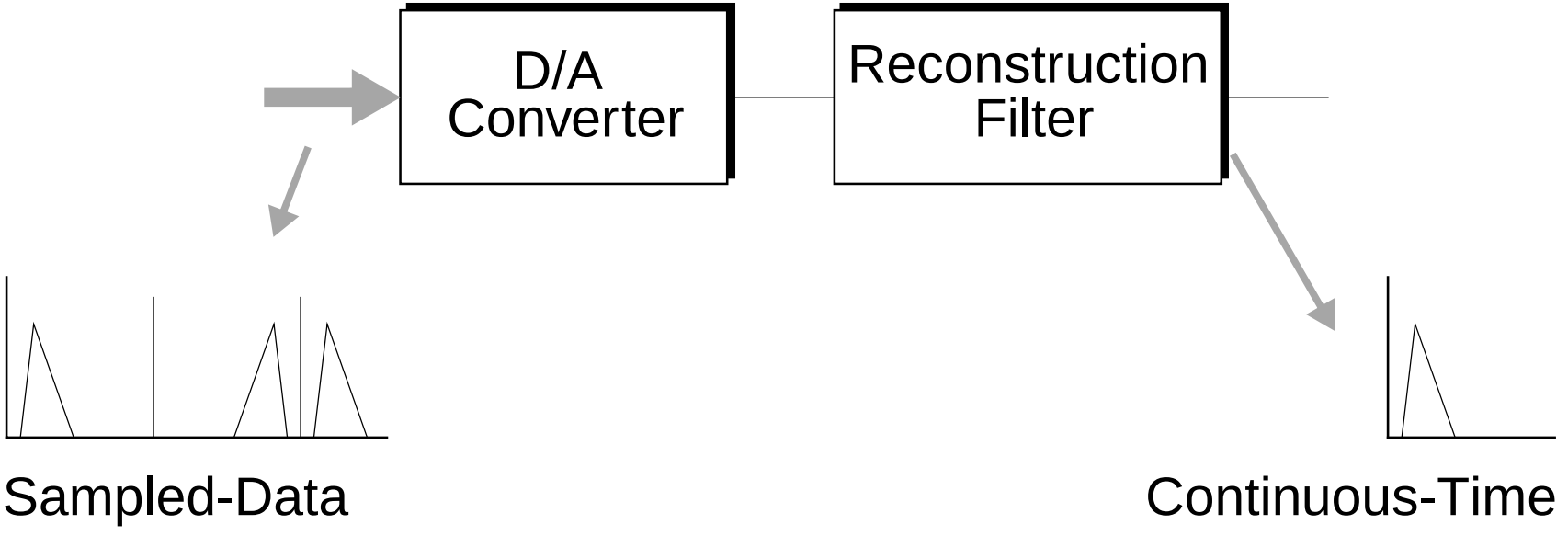
- $Out = 2^{N+1}\frac{In}{\Delta}$
  - ➥ N ➜ Resolution
  - ➥ Δ ➜ Full scale

- Conversion algorithm

$$\begin{cases} U(k+1) = U(k) + [In - (-1)^{Q(k)+1}\Delta/2] \\ U(0) = In \end{cases}, \quad 0 \le k \le 2^N$$

# D/A Conversion Fundamentals

- A D/A converter transforms a digital sampled-data signal into an analog continuous-time signal
  - Domain transformation
  - Reconstruction



# D/A Conversion Fundamentals

- The conversion from digital to analog does not change the spectrum of the signal
- A cardinal hold performs the ideal reconstruction

  $R(\omega) = 1 \quad \text{for} \quad \omega \le \omega_S/2; \quad 0 \quad \text{otherwise}$

  $$r(t) = \frac{\sin(\omega_S t/2)}{\omega_S t/2}$$

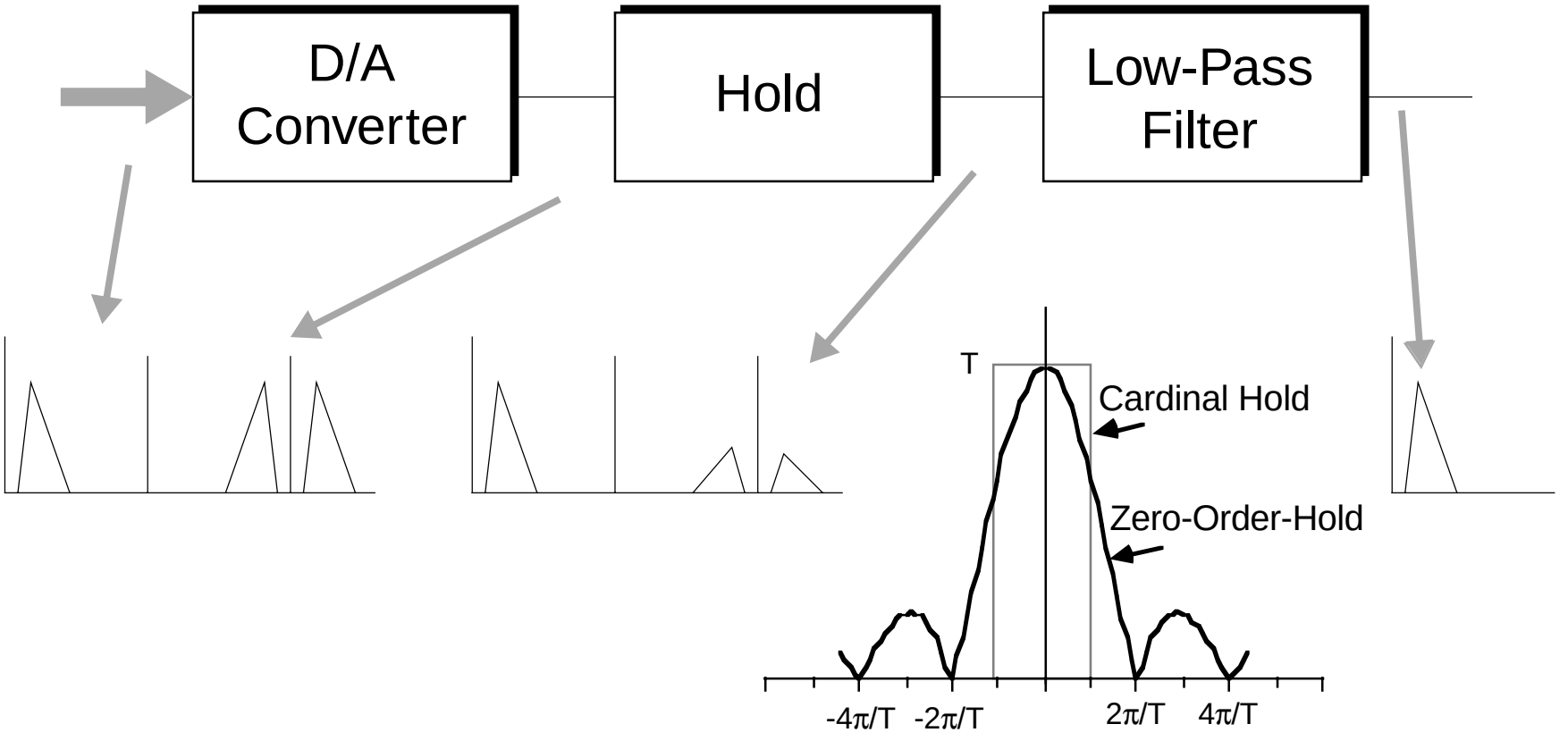
  ☹ The cardinal hold can not be practically realized
- A zero-order hold performs the approximate reconstruction

  $h(t) = 1 \quad \text{for} \quad 0 < t < T; \quad 0 \quad \text{otherwise}$

  $H(\omega) = (1 - e^{j\omega T})/(j\omega)$

# D/A Conversion Fundamentals

- Approximate reconstruction with zero-order hold



# D/A Converter Building Blocks

- The implementation of any conversion algorithm requires active elements and passive components
  - ➥ Measurement or attenuation of analog variables
- Accuracy and stability of attenuation and measurement elements strongly affect the overall performance of the D/A converter
  - ☹ Mismatches are responsible for most of the linearity errors (differential and integral)
- The matching accuracy of integrated resistors is of the order of 0.1%-0.4% ➜ Resolution up to 9-10 bits
  - ➥ Careful layout of the circuit
  - ➥ Interdigitated structures with dummies at the edges

# D/A Converter Building Blocks

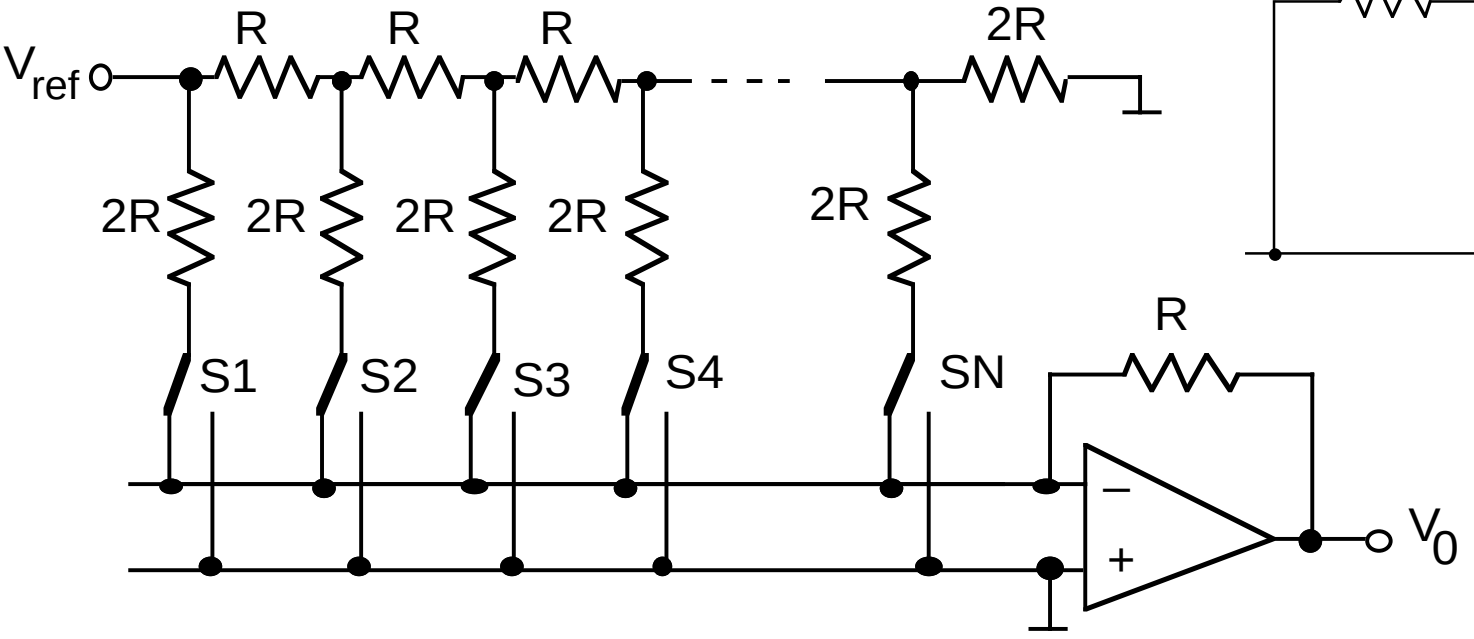
- The matching accuracy of integrated capacitors is of the order of 0.05%-0.2% ➜ Resolution up to 10-12 bits
  - ➥ Careful layout of the circuit
  - ➥ Common centroid structures with dummies at the edges
- Capacitor based D/A converters require analog switches
  - ➥ In CMOS technology switches are easily implemented with a single transistor or a pair of complementary transistors
  - ➥ The on-resistance is inversely proportional to the transistor aspect ratio and on the overdrive voltage applied ($V_{GS} - V_{th}$)
  - ☹ Limitation ➜ Clock feedthrough
- Active elements ➜ Operational amplifiers

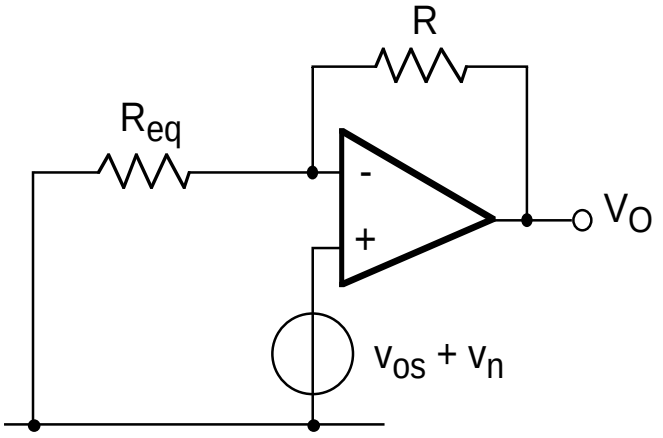
# D/A Converter Architectures

- Resistive and capacitive D/A converters
- Charge redistribution D/A converters
- Multiplying D/A converters
- Algorithmic D/A converters
- Current steering D/A converters
- Sigma-delta D/A converters

# RESISTIVE LADDER D/A CONVERTERS

- The input digital word controls the analog switches

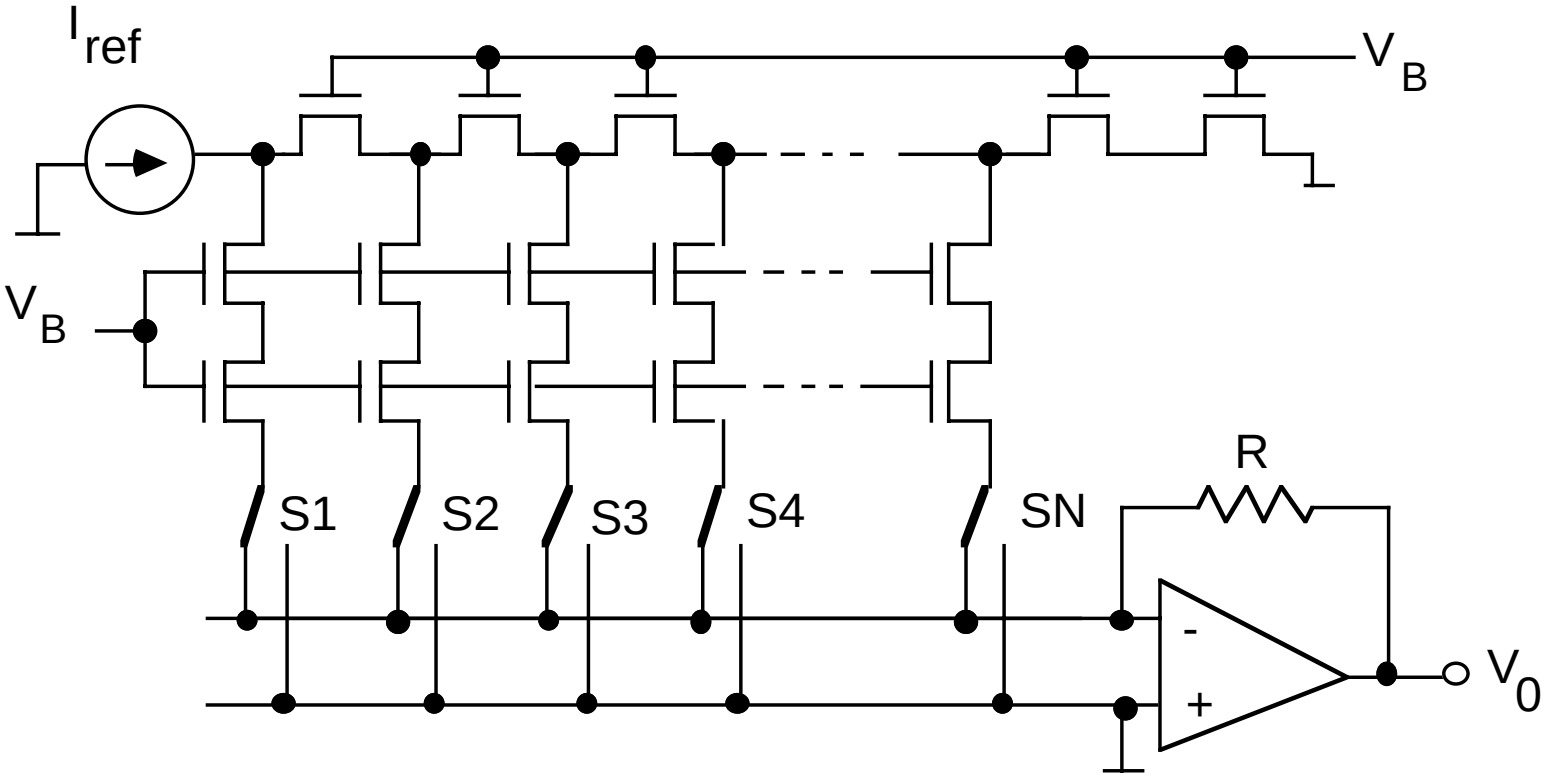



- Limitations ➜ Resistor mismatches and distortion from non-linear amplification of offset and low-frequency noise

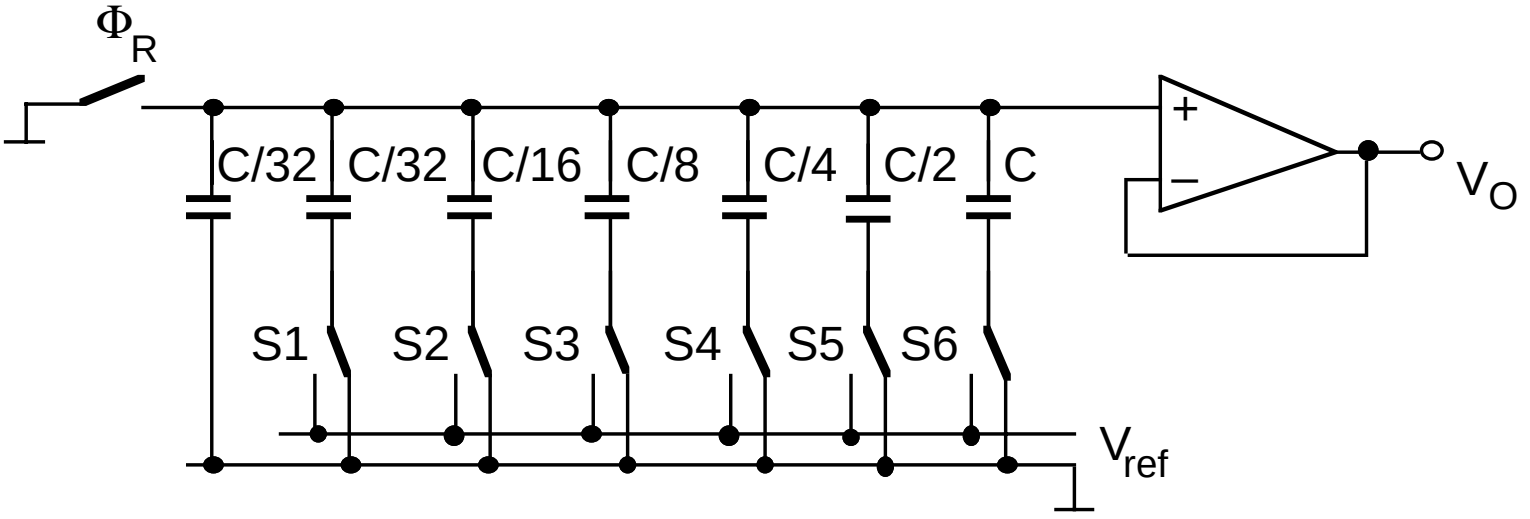
# MOS Current Divider D/A Converters

- Two equal MOS transistors in parallel divide in equal parts the reference current independently of the non-linear response



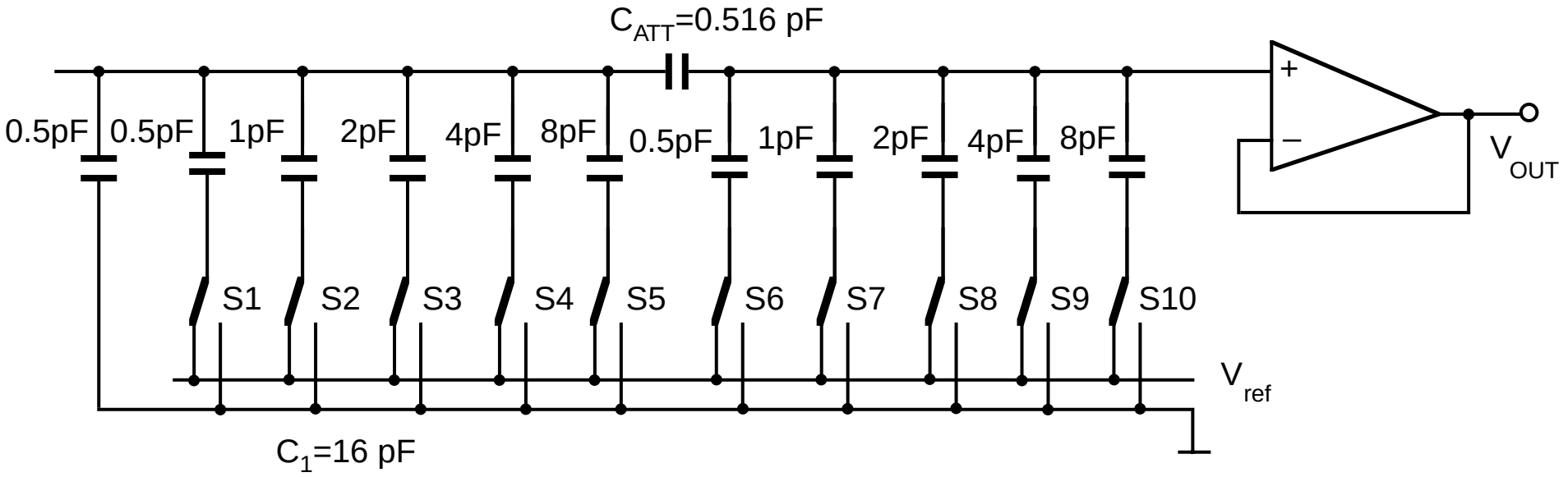

# CAPACITIVE DIVIDER D/A CONVERTERS

- The capacitors are reset ($\Phi_R$) before each conversion
- The input digital word controls the analog switches
- The capacitors are binary weighted
  - ☹ For high resolution the unity capacitance is very small



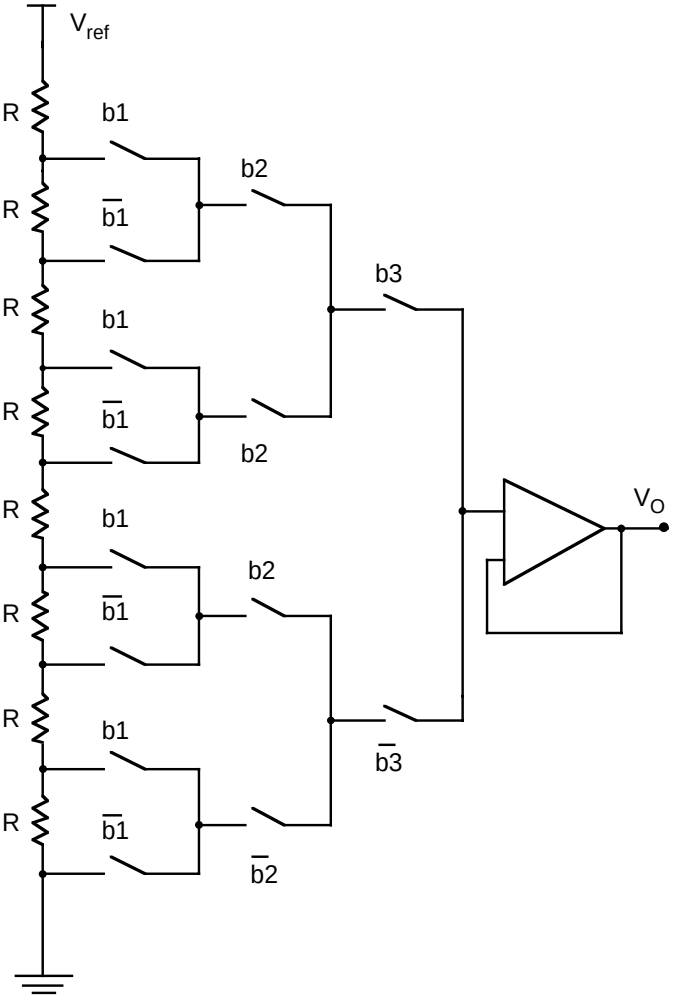
# CAPACITIVE DIVIDER D/A CONVERTERS

- High resolution ➜ Use of an attenuating capacitor
- The unity capacitance is multiplied by a factor k = 32
- Attenuating capacitor ➜ $C_{ATT} = C_1/(k-1)$



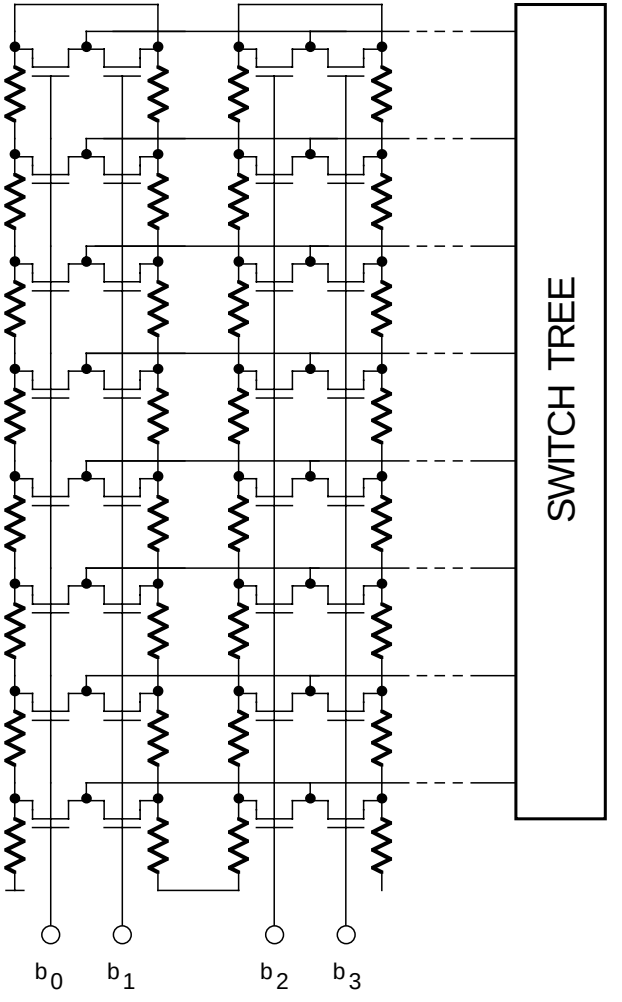
# RESISTIVE DIVIDER D/A CONVERTERS

- The reference voltage is divided by a string of equal resistors
- A particular voltage tap is selected with a tree of switches
- The input impedance of the buffer is very high
- Features
  - ☺ Intrinsically monotonic
  - ☹ Sensitive to the buffer offset
  - ☹ Delay due to several switches in series



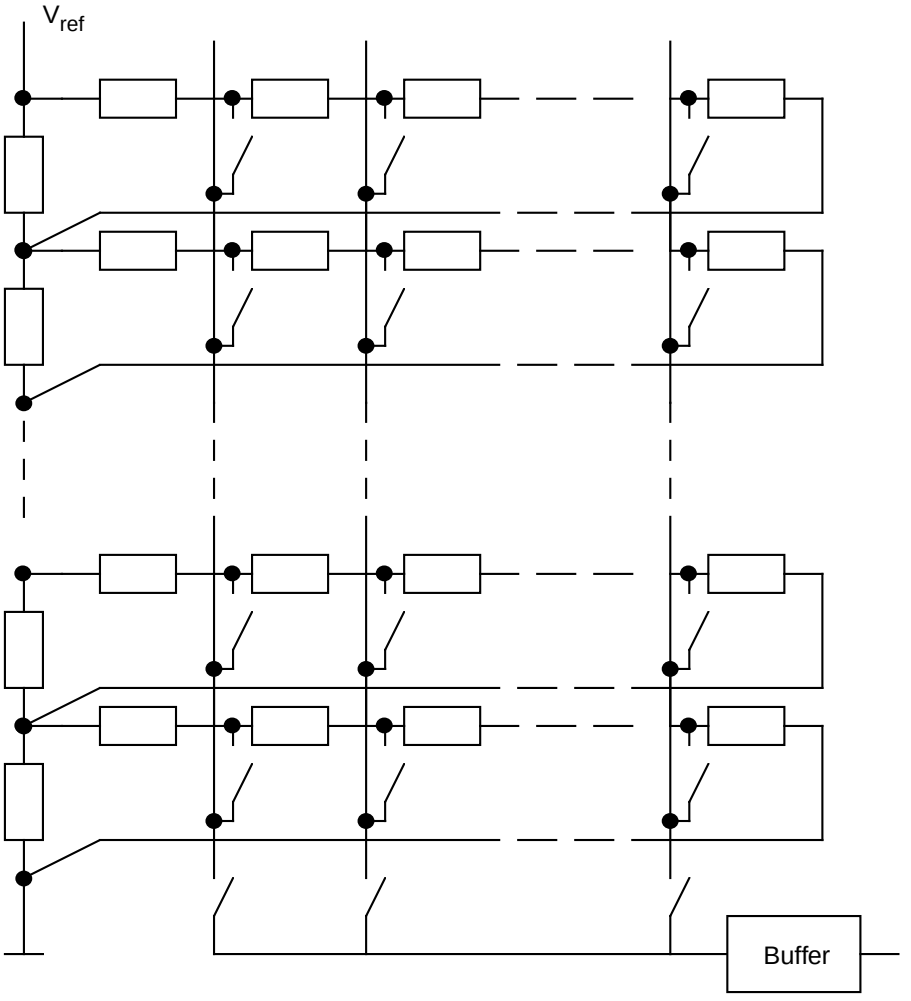
# RESISTIVE DIVIDER D/A CONVERTERS

- Folded resistive string
- Parallel selection of 8 different voltage taps
- Tree of switches to select one of the 8 voltage taps
- Features
  - ☺ Intrinsically monotonic
  - ☹ Corner resistors difficult to implement
  - ☺ Compact layout



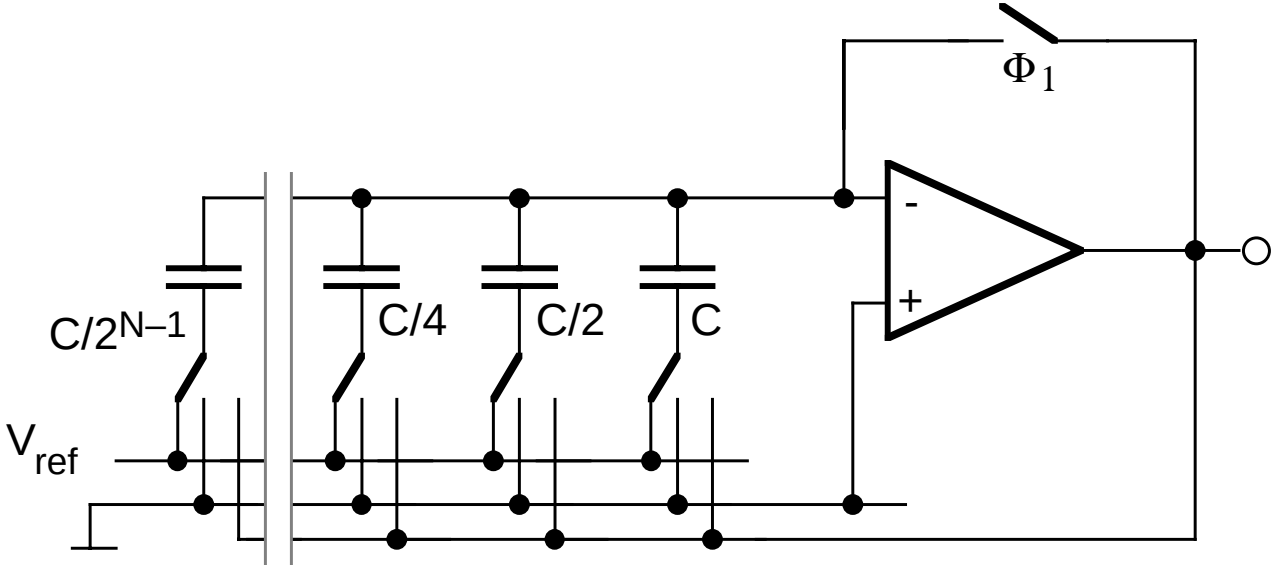
# RESISTIVE DIVIDER D/A CONVERTERS

- Resistor matrix divides the reference voltage (XY selection)
- Output buffer required
- Features
  - ☺ High speed
  - ☺ Intrinsically monotonic
  - ☺ Up to 10 bits of resolution
  - ☹ Limitations due to the output buffer



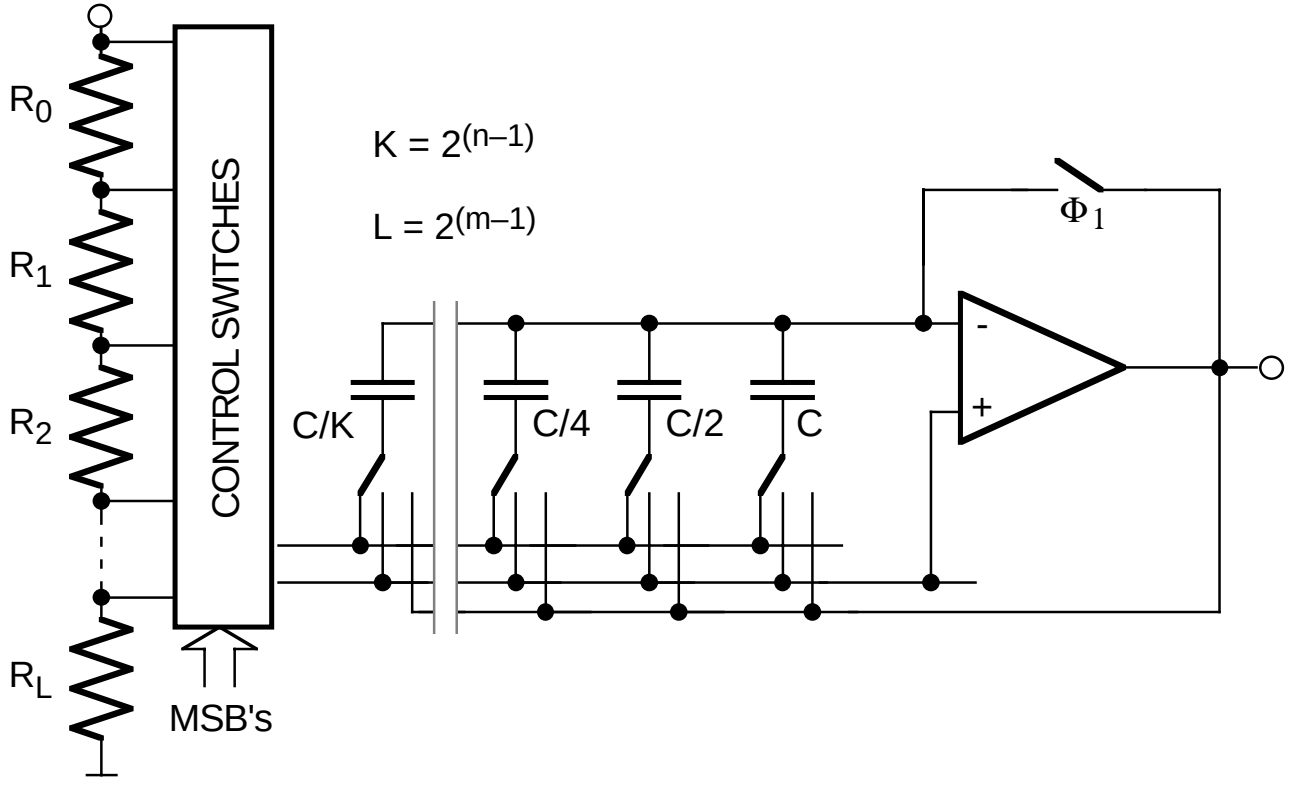
# CHARGE REDISTRIBUTION D/A CONVERTERS

- The charge stored the capacitive array during one clock phase is redistributed in the entire array during the other clock phase
  - ☺ Offset insensitive architecture
  - ☹ Output available only during one clock phase



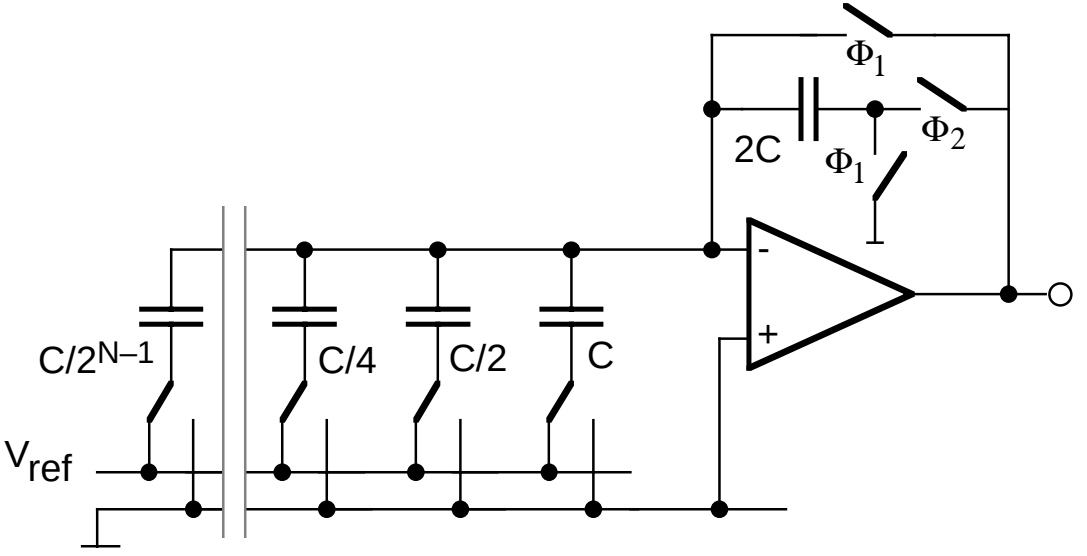
# RESISTIVE AND CAPACITIVE D/A CONVERTERS

- The m MSBs are provided by a resistive divider DAC while the n LSBs are provided by a capacitive charge redistribution DAC



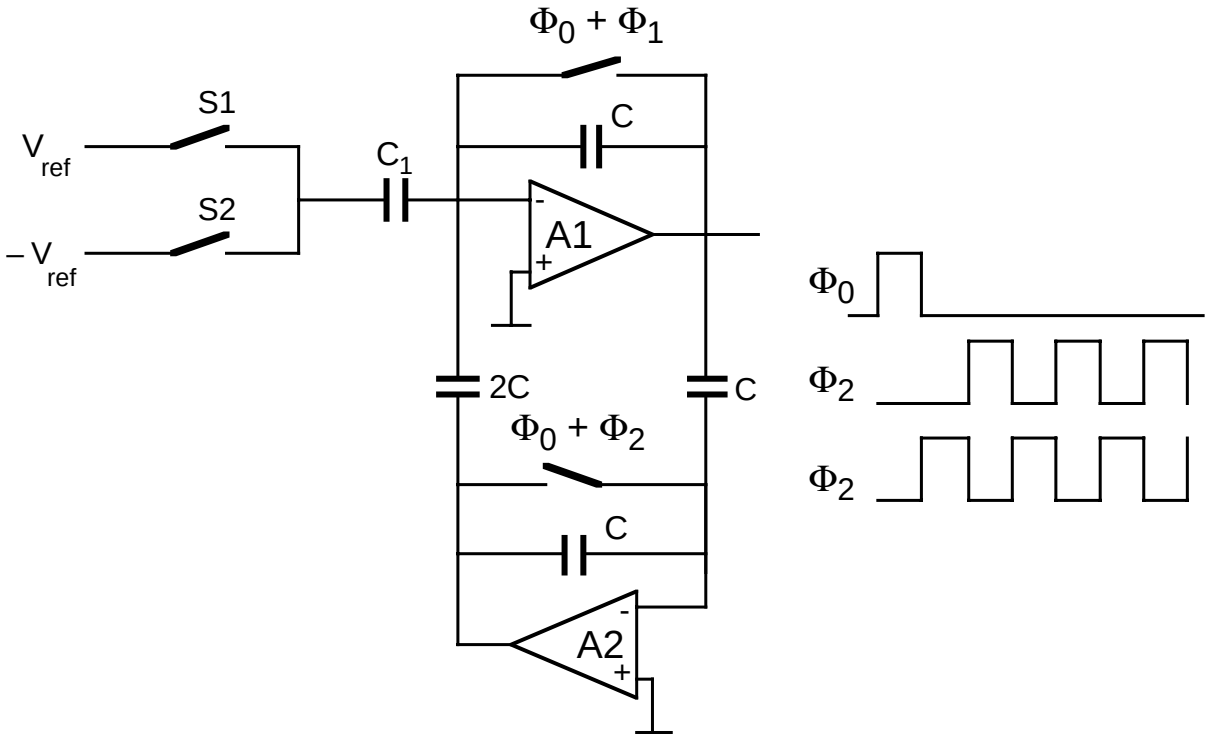
# MULTIPLYING D/A CONVERTER

- The charge stored in the array in one clock phase is injected into the feedback capacitor during the other clock phase
- Features
  - ☺ Inverting or non-inverting
  - ☺ Offset insensitive



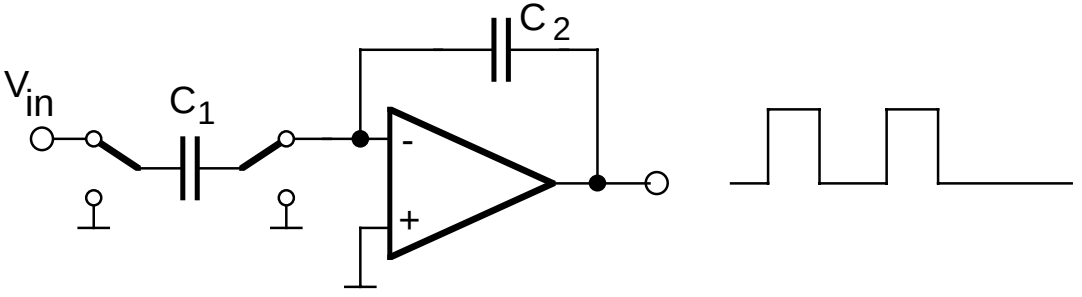

# ALGORITHMIC D/A CONVERTERS

- The analog output is built in N successive clock cycles
- During each clock cycle the voltage in the loop is multiplied by 2

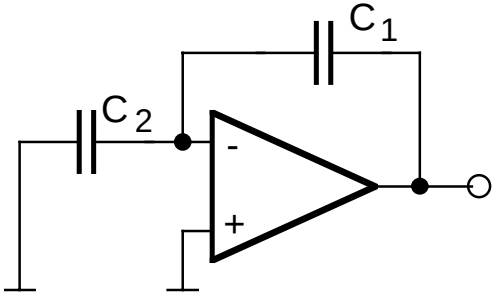


# ALGORITHMIC D/A CONVERTERS

- Exact multiplication by 2
  - Integrate the input signal two times

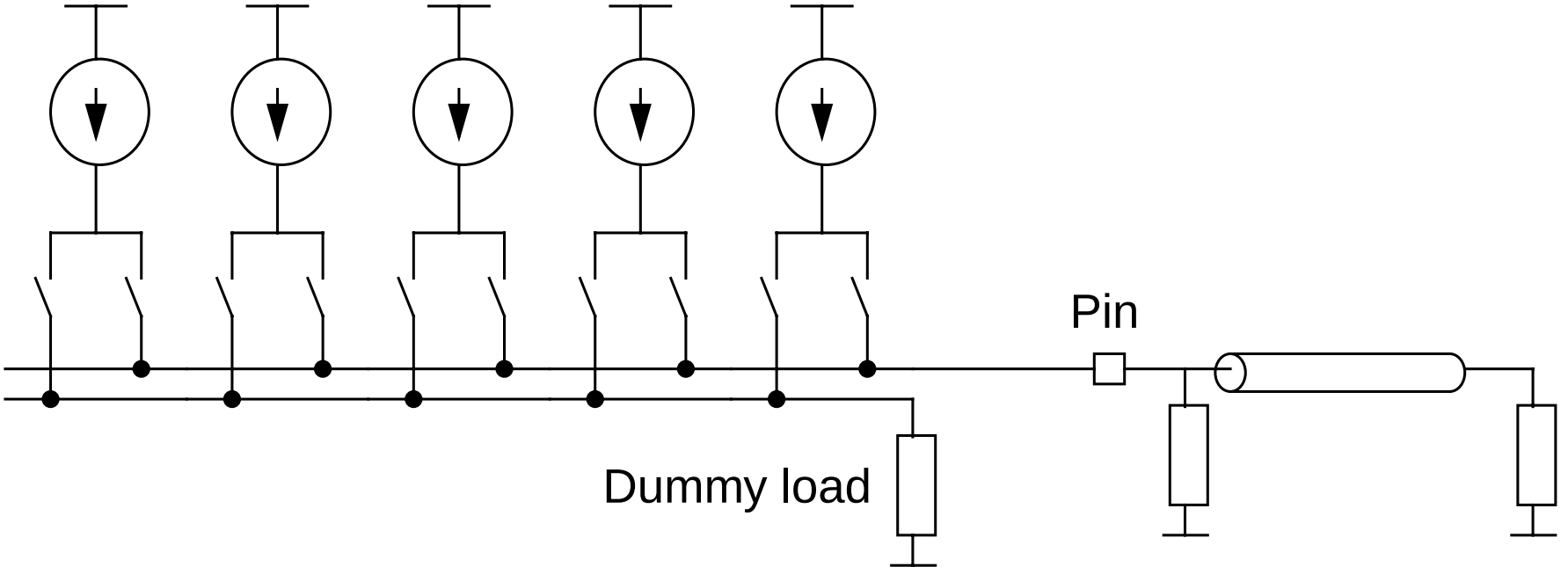



  - Exchange capacitors $C_1$ and $C_2$



# CURRENT STEERING D/A CONVERTERS

- Suitable for very high speed applications (several tens of MHz)
- A current proportional to the input digital word is injected into the external resistive load (termination resistance)



# CURRENT STEERING D/A CONVERTERS

- Current steering D/A converters design issues
  - Binary weighted current sources or equal current sources
  - Switch on and off the current sources ➜ Switching glitches
  - Matching between current sources
- Current steering D/A converters implementation issues
  - Output resistance

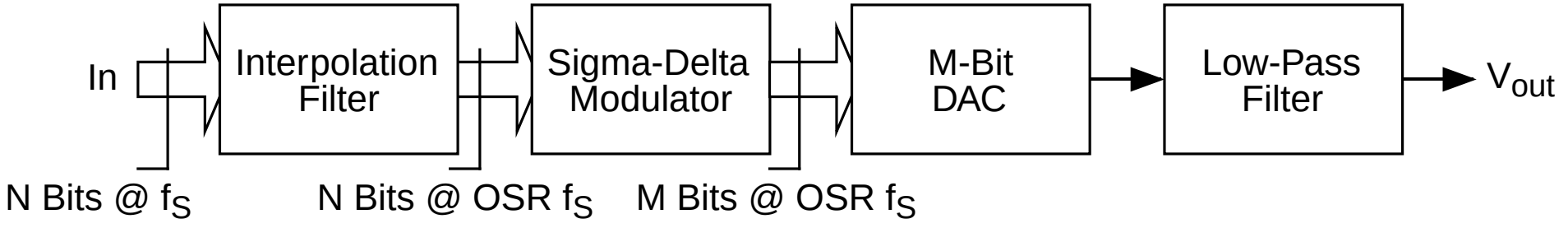
$$I_D = \mu C_{ox}(W/L)(V_{GS} - V_{Th})^2(1 + \lambda V_{DS})$$

$$I_C = I_0 e^{(qV_{BE})/(kT)}(1 + V_{CE}/V_A)$$

  - Voltage drop on the power supply line ➜ Mirror current sources locally and distribute currents

# SIGMA DELTA D/A CONVERTER

- Audio applications (CD players)
- The N-bit input digital word is truncated to M-bits (M < N) and the sampling frequency is increased
  - ➥ Digital interpolation filter and digital sigma-delta modulator
  - ☺ Oversampling and noise-shaping
  - ➥ M-bit D/A converter and reconstruction low-pass filter
- Trade-off between accuracy, speed and complexity



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