Exercise Circ01

Consider a CMOS fabrication process with the following process parameters:

$k_n' = \mu_n C_{ox} = 90\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 30\ \mu A/V^2$,

$V_{th,n} = |V_{th,p}| = 0.6$ V,

$L_{min} = 0.5\ \mu m$ (minimum allowed channel length, for both N-channel and P-channel transistors),

$C_{ox} = 2\ fF/\mu m^2$ (gate oxide capacitance per unit area),

$t_{ox} = 15$ nm (gate oxide thickness).

The transistors in the elementary inverter used in an integrated circuit fabricated with the above process have the following sizes:

n-channel transistor: W_n (channel width) = 2 μm; L_n (channel length) = 0.5 μm;

p-channel transistor: W_p (channel width) = 6 μm; L_p (channel length) = 0.5 μm.

The used fabrication technology and the layout are such that, for each transistor, the drain capacitance and the source capacitance turn out to be equal to 25% and 20%, respectively, of the gate capacitance, whereas the overlap/fringing gate capacitance and the capacitances associated to interconnections are negligible.

Supply voltage V_{DD} is equal to 3 V.

By using seven elementary inverters, we implemented the ring oscillator shown in figure 1.

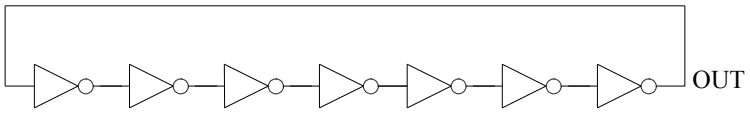

Figure 1

The candidate is asked to:

a) Calculate the delay time of a single inverter within the ring oscillator.

b) Estimate the oscillation frequency of the circuit.