# Exercise Circ02

Consider a *Sea of Gates* whose layout, before drawing interconnections, is shown in the attached figure. Interconnections, implemented in metal1 (first metallization layer), can pass along the horizontal direction above the transistors.

Gate isolation is used.

The following rules are assumed:
spacing between adiacent transistor gates: 1.6 μm;
metal interconnection pitch: 1 μm;
metal1-metal1 spacing: 0.4 μm;
metal1-contact overlap: 0.1 μm;
height ($H_N$) of $N^-$-diffusion: 3 μm;
height ($H_P$) of $P^+$-diffusion: 7.5 μm.

The gate length is 0.4 μm for both N-channel and P-channel transistors.

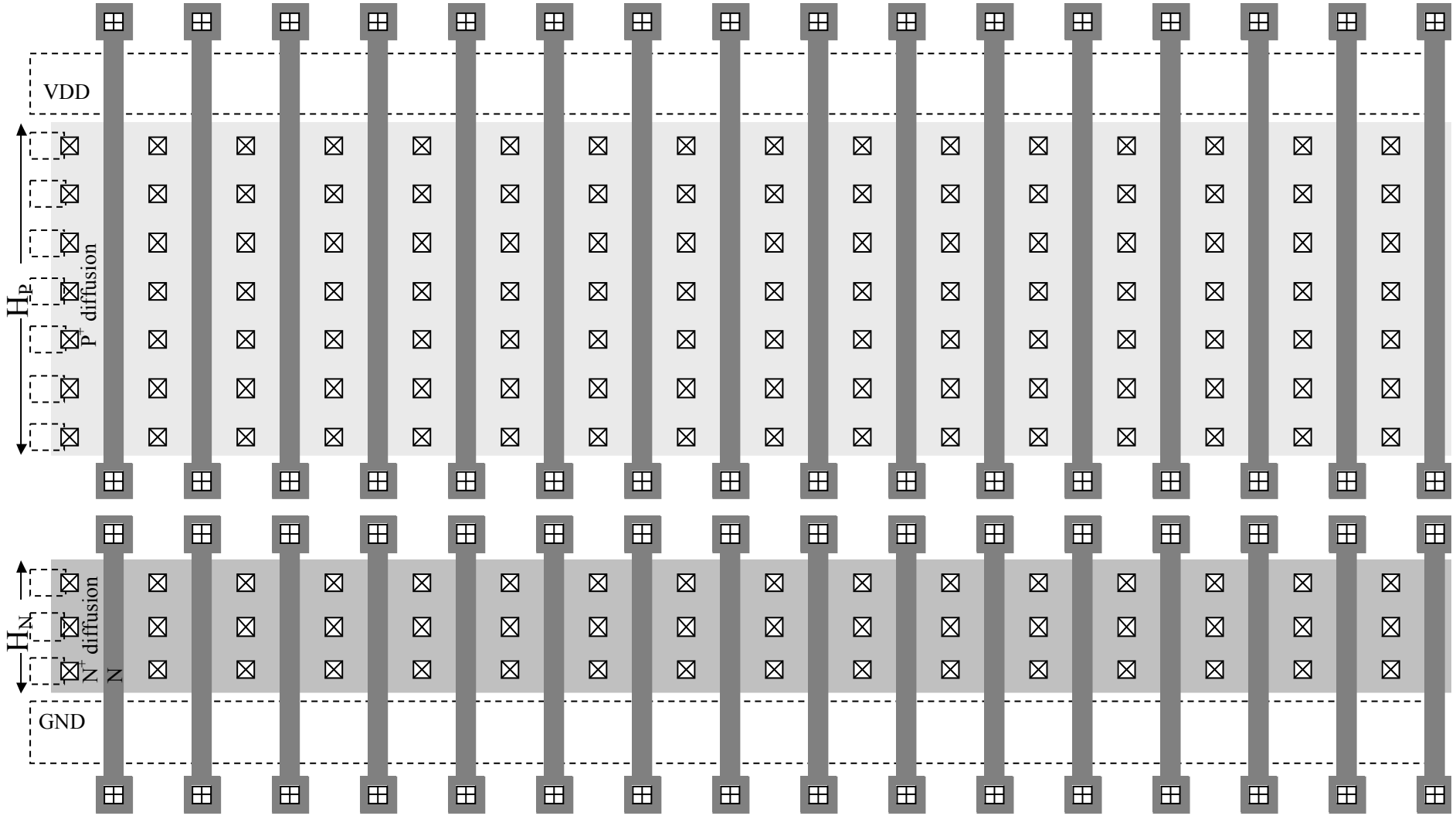
In case design rules non explicitly shown are required to solve the exercise, they can be derived from the layout in the figure, assuming a layout grid with a pitch of 0.1 μm.

The wafer fabrication process of the considered *Sea of Gates* has the following parameters:
$k'_n = \mu_n C_{ox} = 100\,\mu\text{A/V}^2$; $k'_p = \mu_p C_{ox} = 40\,\mu\text{A/V}^2$;
$V_{th,N} = \left|V_{th,P}\right| = 0.7$ V,
$C_{ox}$ = 2.6 fF/μm$^2$,
$t_{ox}$ = 12 nm;
$C_{ja}$ (junction capacitance per unit area) = 0.05 fF/ μm$^2$;
$C_{jsw}$ (junction capacitance per unit perimeter) = 0.02 fF/ μm
(the values of junction capacitance per unit area and per unit perimeter are averaged over the voltage swing from 0 V to VDD and are assumed equal for $N^+$- and $P^+$-regions).

Gate overlap capacitances and interconnection capacitances are assumed to be negligible.

Supply voltage VDD is equal to 3.3 V.

The candidate is asked to design a symmetrical CMOS inverter able to ensure a delay time of about 2 ns (in any case, not higher than 2 ns) in the presence of an overall capacitive load of 3 pF (in nominal conditions) when the input signal has an ideal step 0/1 or 1/0 transistion.




possible position of metal1 lines above $P^+$ or $N^+$ diffusions

possible position of contacts for $P^+$ or $N^+$ diffusions

possible position of contacts for polysilicon