Exercise Circ03

Consider a CMOS fabrication process with the following parameters:

$k_n' = \mu_n C_{ox} = 135\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 45\ \mu A/V^2$,

$V_{th,n} = |V_{th,p}| = 0.6$ V,

$L_{min} = 0.4$ µm (minimjum allowed chanel length),

$t_{ox} = 12$ nm (gate oxide thickness),

$C_{ox} = 2.5$ fF/µm^2 (gate oxide capacitance per unit area),

$C_{ov} = 0.2$ fF/µm (gate overlap capacitance per unit length per each side, including both overlap and fringing effects),

$C_{ja} = 0.25$ fF/µm^2 (junction capacitance per unit area),

$C_{jsw} = 0.1$ fF/µm (junction capacitance per unit perimeter)
(the values of junction capacitance per unit area and per unit perimeter are averaged over the voltage swing from 0 V to VDD and are assumed equal for N^+- and P^+-regions).

Consider now the elementary inverter shown in Figure 1, where we have the following values:

$W_N = 1.6$ µm (channel width for N-channel transistors);

$W_P = 4.8$ µm (channel width for P-channel transistors);

$L_N = L_P = L_{min}$ (channel length for N-channel and P-channel transistors);

A = 1 µm, B = 1.2 µm (in case other design rules, not specifically shown, are required to solve the exercise, they can be derived from the layout in Figure 1, assuming a layout grid with a pitch of 0.1 µm).

Supply voltage $V_{DD} - V_{SS}$ is equal to 3 V.

Lateral diffusion in MOS transistors, as well as any parasitic element non referred to above, can be assumed to be negligible.

A single suitably designed inverter has to be included, as a buffer, between the above elementary inverter and a load capacitor CL equal to 2 pF, as shown in Fig. 2.

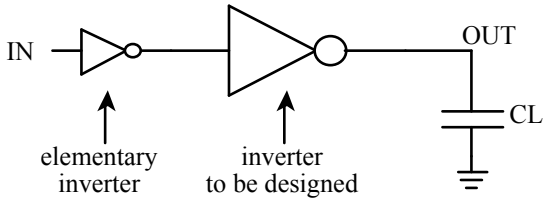

Figure 2

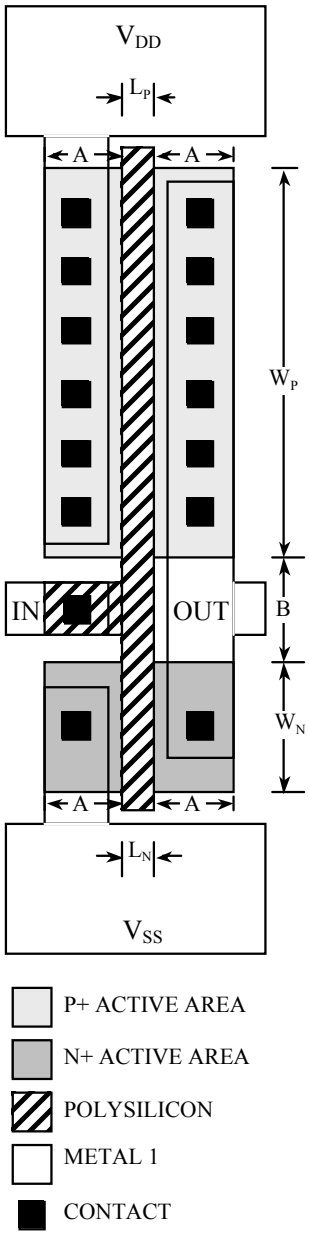

Figure 1

The candidate is asked to:

a) design the buffer inverter so as to minimizet the overall delay time from a transition of input signal IN and the ensuing transition of output signal OUT;

b) calculate the delay time from a transition of input signal IN and the ensuing transition of output signal OUT when the buffer as designed from item a) is used;

c) estimate the average power dissipation of the circuit in Figure 2 when inpit signal IN has the waveform shown in Figure 3*, where T = 4 ns and $t_1 = t_2 = 10$ ps; for this estimation, static power coinsumption can be assumed to be negligible;

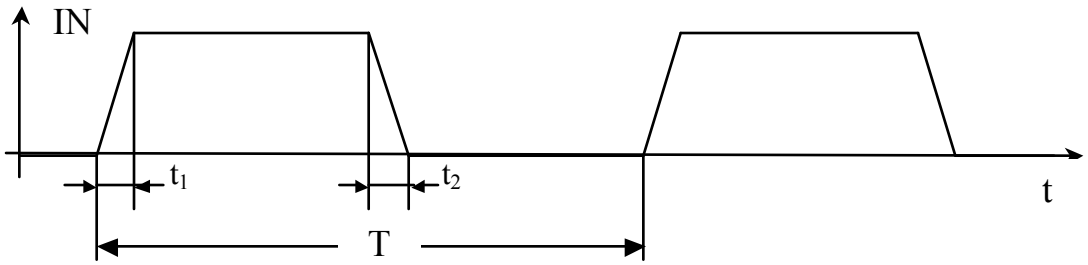

Figure 3

* for the sake of simplicity, Figure 3 is not to scale along the horizontal axis.

d) assume now that a series inductance L = 2 nH is present between the source terminal of the pull-down transistor of the buffer designed as from item a) and ground (V_{SS}), as shown in Fig. 4; the candidate is asked to estimate the noise that arises at the source terminal of the pull-down transistor of the buffer due to a transition 1/0 of output signal OUT, which takes place as a consequence of a transition 1/0 of input signal IN as shown in Fig. 3.

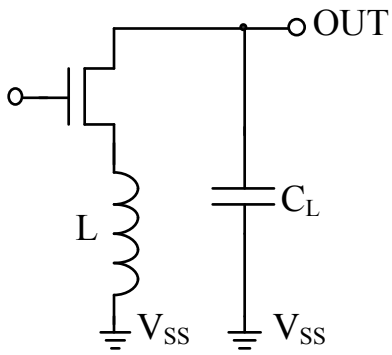

Figure 4