Exercise Circ04

Consider a CMOS fabrication process with the following process parameters:

$k_n' = \mu_n C_{ox} = 150\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 50\ \mu A/V^2$,
$V_{th,n} = |V_{th,p}| = 0.6$ V,
$L_{min} = 0.4\ \mu m$ (minimum allowed channel length, for both N-channel and P-channel transistors),
$C_{ox} = 2.5\ fF/\mu m^2$ (gate oxide capacitance per unit area),
$t_{ox} = 12$ nm (gate oxide thickness).

The used fabrication technology and the layout are such that, for each transistor, the drain capacitance and the source capacitance turn out to be equal to 20% and 25%, respectively, of the gate capacitance. The overlap/fringing gate capacitance and the capacitances associated to interconnections are assumed to be negligible.

Supply voltage V_{DD} is equal to 3 V.

The transistors in the elementary inverter used in an integrated circuit fabricated with the above process have the following sizes:

n-channel transistor: W_n (channel width) = 2 μm; L_n (channel length) = 0.4 μm;
p-channel transistor: W_p (channel width) = 6 μm; L_p (channel length) = 0.4 μm.

A processing chain whose last section is formed bty two elementary inverters has to drive a load capacitor CL equal to 0.4 pF.

The candidate is asked to:

a) calculate the delay time of the cascade of the two elementary inverters when no capacitor CL is connected (Fig. 1.a);
b) calculate the delay time of the cascade of the two elementary inverters when capacitor CL is connected (Fig. 1.b);
c) design a buffer to be included between the output of the processing chain and CL so as to adequately limit the overall delay time in the presence of the load capacitor CL;
d) estimate the delay time from the input IN of the cascade of the two elementary inverters and node OUT when the designed buffer (as from item c) is used to drive CL.

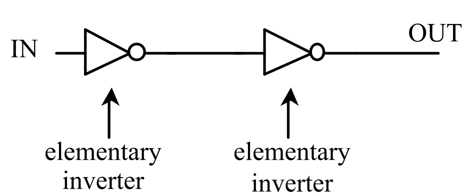

Figure 1.a

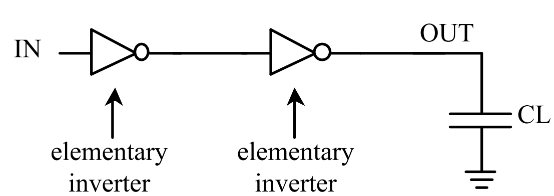

Figure 1.b

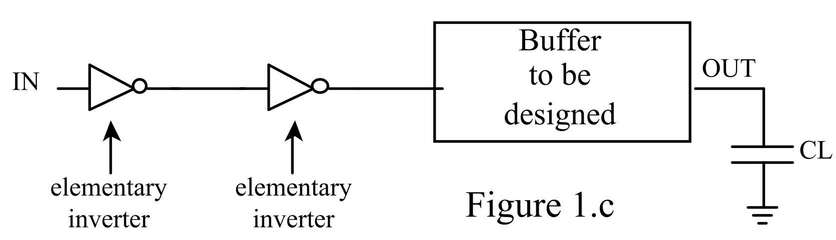

Figure 1.c