Exercise Circ05

Consider a CMOS fabrication process with the following process parameters:

$k_n' = \mu_n C_{ox} = 90\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 30\ \mu A/V^2$,
$V_{th,n} = |V_{th,p}| = 0.75$ V,
$L_{min} = 0.6\ \mu m$ (minimum allowed channel length, for both N-channel and P-channel transistors),
$C_{ox} = 2\ fF/\mu m^2$ (gate oxide capacitance per unit area),
$t_{ox} = 15$ nm (gate oxide thickness).

The source and drain capacitances of the transistors in the considered technology are assumed to be negligible with respect to the gate capacitance. The overlap/fringing gate capacitance and the capacitances associated to interconnections are also assumed to be negligible.

Supply voltage V_{DD} is equal to 3 V.

The transistors in the elementary inverter used in an integrated circuit fabricated with the above process have the following sizes:

n-channel transistor: W_n (channel width) = 10 μm; L_n (channel length) = 0.6 μm;
p-channel transistor: W_p (channel width) = 30 μm; L_p (channel length) = 0.6 μm.

A processing chain consisting of the cascade of elementary inverters has to drive a load capacitor CL equal to 2.5 pF.

The candidate is asked to:

a) calculate the delay time of one elementary inverter within the above processing chain;
b) design a buffer to be included between the output of the processing chain and CL so as to adequately limit the overall delay time in the presence of the load capacitor CL;
c) estimate the delay time from the input IN of the last inverter of the processing chain and buffer output when the designed buffer (as from item b) is used to drive CL.