Exercise Circ06

Consider a CMOS fabrication process with the following process parameters:

$k_n' = \mu_n C_{ox} = 120\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 40\ \mu A/V^2$,

$V_{th,n} = |V_{th,p}| = 0.5$ V,

$L_{min} = 0.4\ \mu m$ (minimum allowed channel length, for both N-channel and P-channel transistors),

$C_{ox} = 2\ fF/\mu m^2$ (gate oxide capacitance per unit area),

$t_{ox} = 15$ nm (gate oxide thickness).

The used fabrication technology and the layout are such that, for each transistor, the drain capacitance and the source capacitance turn out to be equal to 20% and 30%, respectively, of the gate capacitance, whereas the overlap/fringing gate capacitance and the capacitances associated to interconnections are negligible.

The transistors in the elementary inverter used in an integrated circuit fabricated with the above process have the following sizes:

n-channel transistor: W_n (channel width) = 3 μm; L_n (channel length) = 0.4 μm;

p-channel transistor: W_p (channel width) = 9 μm; L_p (channel length) = 0.4 μm.

Supply voltage V_{DD} is equal to 3 V.

By using NAND gates (connected as shown), we implemented the circuit illustrated in Fig. 1, which is a ring oscillator, where an additional NAND (identical to the above NAND gates) is added to drive the output capacitor CL = 0.4 pF. The widths (W) of P-channel and N-channel transistors in the NAND gates (15 μm and 10 μm, respectively) are shown in the figure; the channel length (L) of all transistors is 0.4 μm.

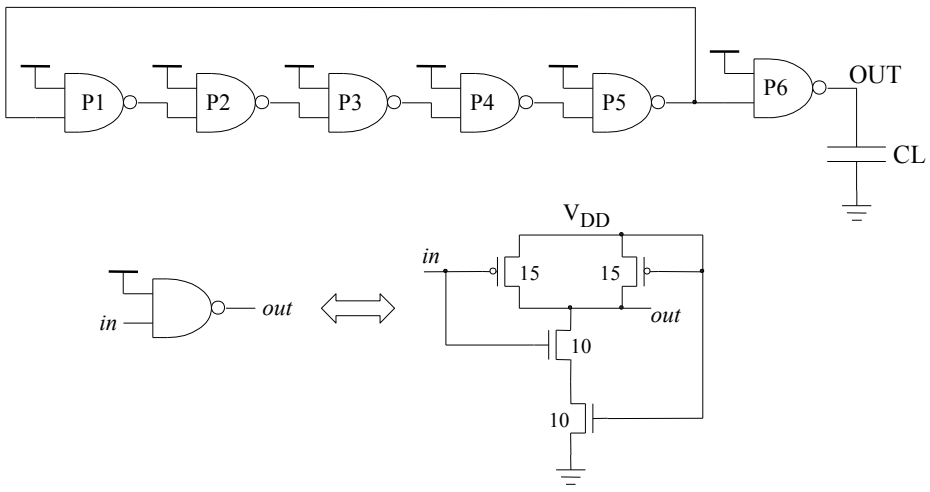

Figure 1

The candidate is asked to:

A. Calculate the delay time of NAND gate P6, justifying all assumptions made, if any.

B. Calculate the delay time of NAND gate P1, justifying all assumptions made, if any.

C. Estimate the oscillation frequency of the circuit.

D. Estimate the oscillation frequency of the circuit when each NAND gate is replaced by the above elementary inverter.