Exercise Circ07

Consider a CMOS fabrication process with the following process parameters:

$k_n' = \mu_n C_{ox} = 120\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 40\ \mu A/V^2$,

$V_{th,n} = |V_{th,p}| = 0.6$ V,

$L_{min} = 0.40\ \mu m$ (minimum allowed channel length) for both N-channel and P-channel transistors,

$C_{ox} = 2$ fF/μm^2 (gate capacitance per unit area),

$t_{ox} = 15$ nm (gate oxide thickness).

The used fabrication technology and the layout are such that, for each transistor, the drain capacitance and the source capacitance turn out to be equal to 20% and 25%, respectively, of the gate capacitance, whereas the overlap/fringing gate capacitance and the capacitances associated to interconnections are negligible.

Supply voltage V_{DD} is equal to 3 V.

The transistors in the elementary inverter used in an integrated circuit fabricated with the above process, have the following sizes:

N-channel transistor: channel width $W_n = 2.5\ \mu m$; channel length $L_n = 0.4\ \mu m$;

P-channel transistor: channel width $W_p = 7.5\ \mu m$; channel length $L_p = 0.4\ \mu m$.

As shown in Figure 1, a single inverter has to be included, as a buffer, between the above elementary inverter and a capacitive load C_L equal to 0.8 pF (which represents the input capacirtance of a cascaded digtal network).

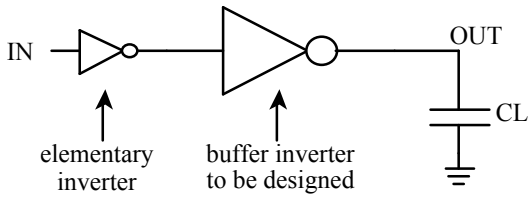

Figure 1

The candidate is asked to design the buffer inverter so as adequately limit the overall delay time from node IN to node OUT.