Exercise Circ08

The layout a *Sea of Gates*, before drawing interconnections, is shown in the attached figure. Interconnections, implemented in metal1 (first metallization layer), can pass along the horizontal direction above the transistors.

Gate isolation is used.

The following rules are assumed:
spacing between adiacent transistor gates: 1.6 mm;
metal interconnection pitch: 1 mm;
metal1-metal1 spacing: 0.4 mm;
metal1-contact overlap: 0.1 mm;
height (H_N) of N^--diffusion: 3 mm;
height (H_P) of P^+-diffusion: 7.5 mm.

The gate length is 0.4 mm for both N-channel and P-channel transistors.

In case design rules non explicitly shown are required to solve the exercise, they can be derived from the layout in the figure, assuming a layout grid with a pitch of 0.1 μm.

The wafer fabrication process of the considered *Sea of Gates* has the following parameters:

$k_n' = \mu_n C_{ox} = 150\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 60\ \mu A/V^2$,

$V_{th,n} = |V_{th,p}| = 0.7$ V,
$C_{ox} = 2.8$ fF/mm^2,
$t_{ox} = 9$ nm;
C_{ja} (junction capacitance per unit area) = 0.04 fF/ mm^2;
C_{jsw} (junction capacitance per unit perimeter) = 0.01 fF/ mm
(the values of junction capacitance per unit area and per unit perimeter are averaged over the voltage swing from 0 V to VDD and are assumed equal for N^+- and P^+-regions).

Gate overlap capacitances and interconnection capacitances are assumed to be negligible.

Supply voltage VDD is equal to 3.3 V.

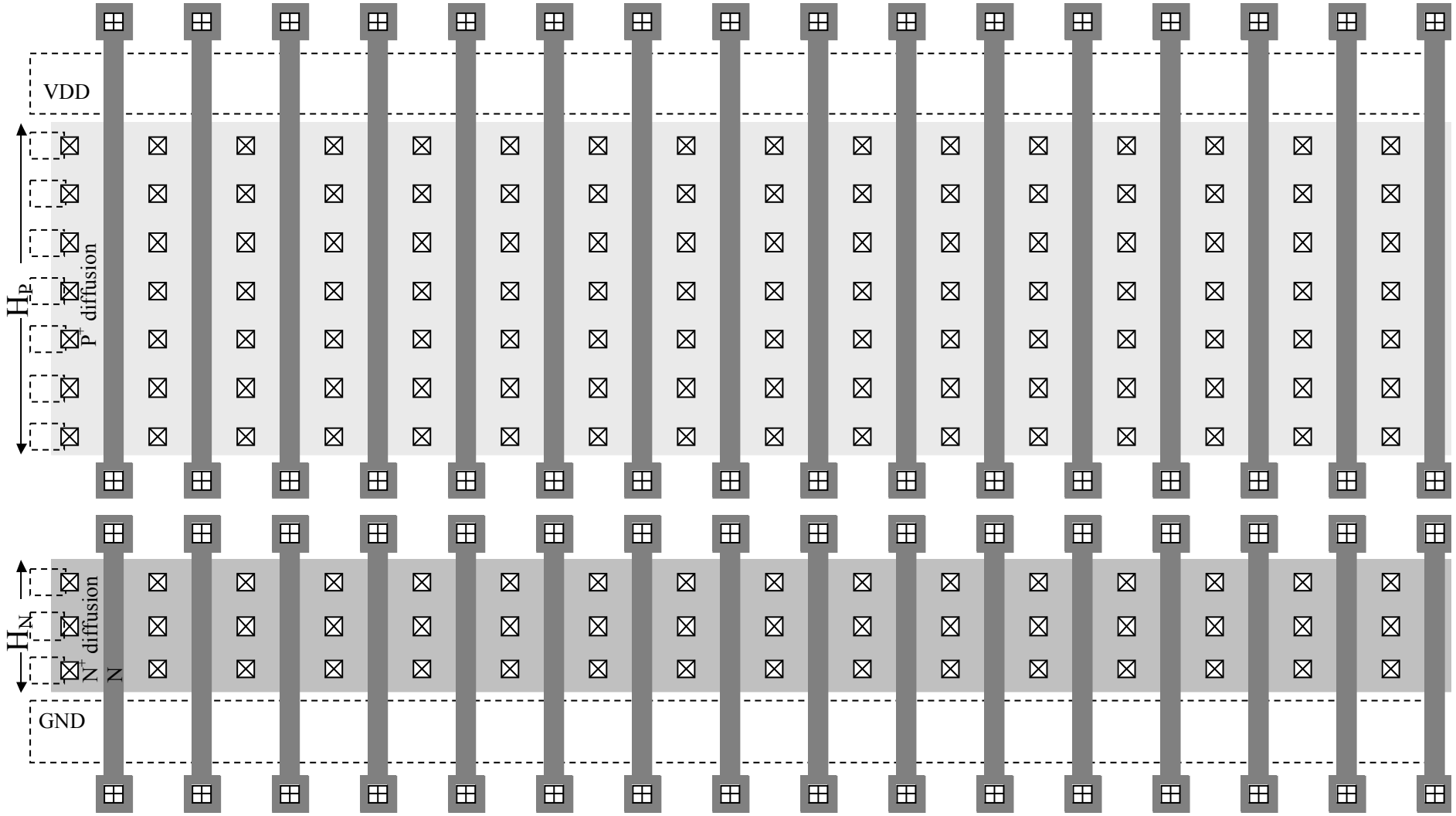
The transistors of the elementary inverter in an integrated circuit based on the above Sea of Gates have the following dimensions: :
N-channel transistor: $W_N = 3$ mm; $L_N = 0.4$ mm;
P-channel transistor: $W_P = 7.5$ mm; $L_P = 0.4$ mm.

The candidate is asked to

A. calculate the delay time of an elementary inverter that drives an external load capacitance C_L = 250 fF;

B. design a buffer, implemented by means of the considered *Sea of Gates*, to be placed between the above elementary inverter and the load capacitor C_L, so as to adequately limit the delay time from the input of the elementary inverter and C_L;

C. calculate the delay from the input of the elementary inverter and the output of the designed buffer in the presence of the capacitive load C_L.


VDD
H_P
P^+ diffusion
H_N
N^+ diffusion
N
GND
possible position of metal1 lines above P^+ or N^+ diffusions
possible position of contacts for P^+ or N^+ diffusions
possible position of contacts for polysilicon