Exercise Circ10

Consider a CMOS fabrication process with the following process parameters:

$k_n' = \mu_n C_{ox} = 90\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 40\ \mu A/V^2$,

$V_{th,n} = |V_{th,p}| = 0.5$ V,

$L_{min} = 0.4\ \mu m$ (minimum allowed channel length, for both N-channel and P-channel transistors),

$C_{ox} = 2$ fF/μm^2 (gate oxide capacitance per unit area),

$t_{ox} = 15$ nm (gate oxide thickness).

The used fabrication technology and the layout are such that, for each transistor, the drain capacitance and the source capacitance turn out to be equal to 20% and 25%, respectively, of the gate capacitance, whereas the overlap/fringing gate capacitance and the capacitances associated to interconnections are negligible.

Supply voltage V_{DD} is equal to 3 V.

The transistors in the elementary inverter used in an integrated circuit fabricated with the above process have the following sizes:

n-channel transistor: W_n (channel width) = 3 μm; L_n (channel length) = 0.4 μm;

p-channel transistor: W_p (channel width) = 9 μm; L_p (channel length) = 0.4 μm.

By using the above elementary inverter, we implemented the circuit shown in figure 1, which is a ring oscillator where an elementary inverter (equal to the above elementary inverter) is added to drive the output capacitor C_L = 0.4 pF.

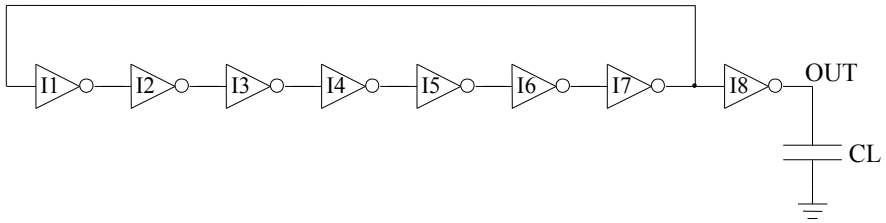

Figure 1

The candidate is asked to:

a) Calculate the delay time of inverter I8, justifying all the assumptions made, if any.

b) Calculate the delay time of the elementary inverters Ii (I = 1 to 7), justifying all the assumptions made, if any.

c) Estimate the oscillation frequency of the circuit.