Exercise Circ11

Consider a CMOS fabrication process with the following process parameters:

$k_n' = \mu_n C_{ox} = 120\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 40\ \mu A/V^2$,

$V_{th,n} = |V_{th,p}| = 0.6$ V,

$L_{min} = 0.4\ \mu m$ (minimum allowed channel length, for both N-channel and P-channel transistors),

$W_{min} = 1.0\ \mu m$ (minimum allowed channel width, for both N-channel and P-channel transistors),

$C_{ox} = 2\ fF/\mu m^2$ (gate oxide capacitance per unit area),

$t_{ox} = 15$ nm (gate oxide thickness).

Supply voltage V_{DD} is equal to 3 V.

The candidate is asked to design a CMOS inverter able to ensure a delay time equal to 1 ns when driving an overall load capacitance of 2 pF (in nominal conditions) in the presence of an ideal step transistion (0/1 or 1/0) at the input node.

Reasonable assumptions should be made for unknown parameters, if any.