Exercise Circ12

Consider a CMOS fabrication process with the following process parameters:

$k_n' = \mu_n C_{ox} = 125\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 50\ \mu A/V^2$,

$V_{th,n} = |V_{th,p}| = 0.6$ V,

$L_{min} = 0.40\ \mu m$ (minimum allowed channel length) for both N-channel and P-channel transistors,

$C_{ox} = 2.4$ fF/μm^2 (gate capacitance per unit area),

$t_{ox} = 10$ nm (gate oxide thickness).

The transistors in the elementary inverter used in an integrated circuit fabricated with the above process have the following sizes:

N-channel transistors: channel width $W_n = 2\ \mu m$; channel length $L_n = 0.4\ \mu m$;

P-channel transistors: channel width $W_p = 5\ \mu m$; channel length $L_p = 0.4\ \mu m$.

The drain capacitance and the source capacitance in each inverter are assumed negligible with respect to the gate capacitance. Overlap/fringing gate capacitance and capacitances associated to interconnections are also assumed to be negligible.

Supply voltage V_{DD} is equal to 3 V.

A processing chain consisting of the cascade of elementary inverters such as the above one has to drive an output capacitive load, C_L, of 3 pF.

The candidate is asked to:

a) calculate the delay time of an inverter within the above processing chain (consisting of only elementary inverters);
b) design a buffer to be placed between the ouput of the last inverter of the above processing chain and the above load capacitor C_L (3 pF) so as to adequately limit the overall delay time when driving C_L;
c) calculate the delay from the input of the last inverter of the processing chain and the output of the designed buffer in the presence of the capacitive load C_L.