Exercise Circ13

Consider a CMOS fabrication process with the following process parameters:

$k_n' = \mu_n C_{ox} = 120\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 40\ \mu A/V^2$,

$V_{th,n} = |V_{th,p}| = 0.6$ V,

$L_{min} = 0.35\ \mu m$ (minimum allowed channel length for both N-channel and P-channel transistors),

$C_{ox} = 2.5$ fF/μm^2 (gate capacitance per unit area),

$t_{ox} = 12$ nm (gate oxide thickness).

Supply voltage V_{DD} is equal to 3 V.

The transistors in the elementary inverter used in the circuit shown in Figure 1, fabricated with the above process, have the following sizes:

N-channel transistors: channel width $W_n = 3.5\ \mu m$; channel length $L_n = 0.35\ \mu m$;

P-channel transistors: channel width $W_p = 7\ \mu m$; channel length $L_p = 0.35\ \mu m$.

The used fabrication technology and the layout are such that, for each transistor, the drain capacitance and the source capacitance turn out to be equal to 20% and 25%, respectively, of the gate capacitance, whereas the overlap/fringing gate capacitance and the capacitances associated to interconnections are negligible.

By using the above elementary inverter, we implemented the circuit shown in figure 1, which is a ring oscillator where elementary inverters (equal to the above elementary inverter) are added to drive output lines.
Capacitor C_L, which represents the load at node OUT, is equal to 0.8 pF.

The candidate is asked to:

a) calculate the delay time of the elementary inverter in the circuit schematic in figure 1, justifying all the assumptions made, if any;

b) estimate the oscillation frequency of the circuit in figure 1;

c) calculate the rise time at node OUT and provide comments.

Attention *- The following point d) is to be solved only provided that the above points a), b), and c) have been completely solved.*

d) Assume that the supply voltage VDD can vary in the range from 2.7 V to 3.3 V and the threshold voltages $V_{th,n}$ and $|V_{th,p}|$ can vary in the range from 0.55 V and 0.65 V. The candidate is asked to calculate the minimum and the maximum oscillation frequency of the circuit in figure 1.

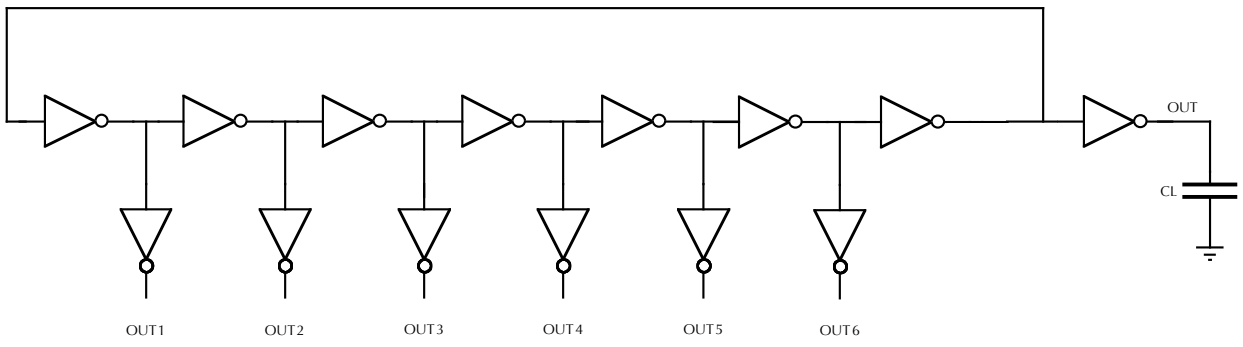

Figure 1