Exercise Circ14

Consider a CMOS fabrication process with the following process parameters:

$k_n' = \mu_n C_{ox} = 90\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 30\ \mu A/V^2$,

$V_{th,n} = |V_{th,p}| = 0.6$ V,

$L_{min} = 0.5\ \mu m$ (minimum allowed channel length for both N-channel and P-channel transistors),

$C_{ox} = 2.0$ fF/μm^2 (gate capacitance per unit area),

$C_{ov} = 0.15$ fF/μm (gate overlap capacitance per unit length per each side, including both overlap and fringing effects),

$t_{ox} = 15$ nm (gate oxide thickness).

Supply voltage V_{DD} is equal to 3 V.

The transistors in the elementary inverter used in the circuit shown in Figure 1, fabricated with the above process, have the following sizes:

N-channel transistors: channel width $W_n = 2\mu m$; channel length $L_n = 0.5\ \mu m$;

P-channel transistors: channel width $W_p = 6\ \mu m$; channel length $L_p = 0.5\ \mu m$.

The used fabrication technology and the layout are such that, for each transistor, the drain capacitance and the source capacitance turn out to be equal to 20% of the gate capacitance, whereas the capacitances associated to interconnections are negligible.

As shown in Figure 1, a buffer stage made up of 2 suitably sized inverters has to be included between the above elementary inverter and a capacitive load C_L equal to 3 pF.

The candidate is asked to:

a) determine the sizes of inverters 1 and 2 in such a way that the delay time between the switching of the input signal IN and the ensuing switching of signal OUT is substantially minimum;

b) calculate the delay between the transition 0/1 of input signal IN and the ensuing transition 1/0 of the output signal OUT when the buffer stage designed in the above point a) is used.

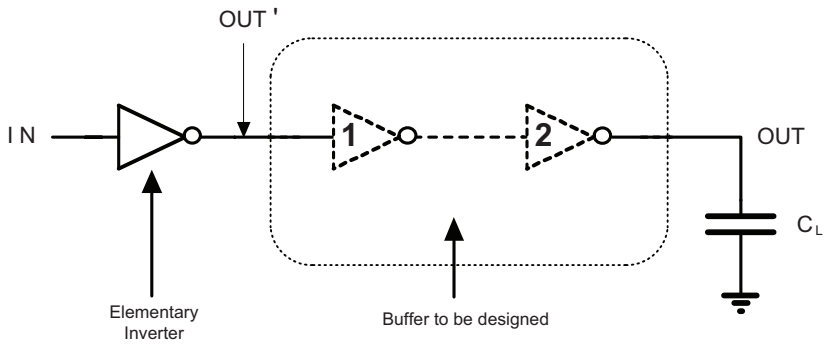

Figure 1

Let us now assume that a series inductance of 2 nH and a series resistance of 2 Ω are present between the source of the pull down transistor (M_D) of the last inverter of the buffer and ground (Figure 2).

c) The candidate is asked to estimate the noise that arises at the source termial of M_D during a transition 1/0 of the output signal OUT as a consequence of a transition 0/1 of the input signal IN of Figure 1.

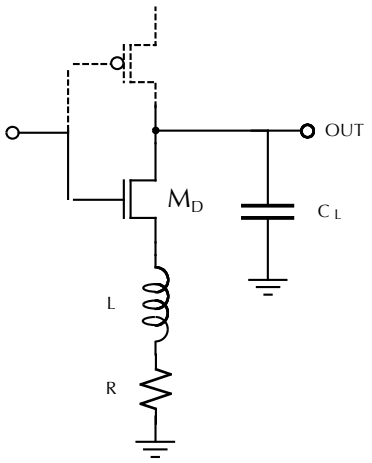

Figure 2

Attention *- The following point d) is to be solved only provided that the above points a), b), and c) have been completely solved.*

Assume now that a capacitor, C_{EXT}, equal to 0.5 pF is connected to node OUT' of the circuit in Figure 1 by means of a complementary CMOS switch (Figure 3);
Input signal IN is connected to V_{DD} (3 V). The driving signals of the CMOS switch are initially s = 0 V, s_{NEG} = 3 V. Capacitor C_{EXT} is initially charged to VDD (3 V). The on-resistance, R_{on}, of the CMOS switch is assumed to be equal to 50 Ω (for simplicity, R_{on} is assumed to be constant over the whole range of signals at nodes OUT' and EXT). All parasitic capacitances associated to the switch are assumed to be negligible.
At t = 1 ns, driving signals s and s_{NEG} are brought to s = 3 V and s_{NEG} = 0 V.

d) The candidate is asked to draw the evolution, over time, of voltages at nodes OUT' and EXT after t = 1ns (approximate time and voltage scales should also be indicated). Switching times of signals s and s_{NEG} are assumed to be zero.

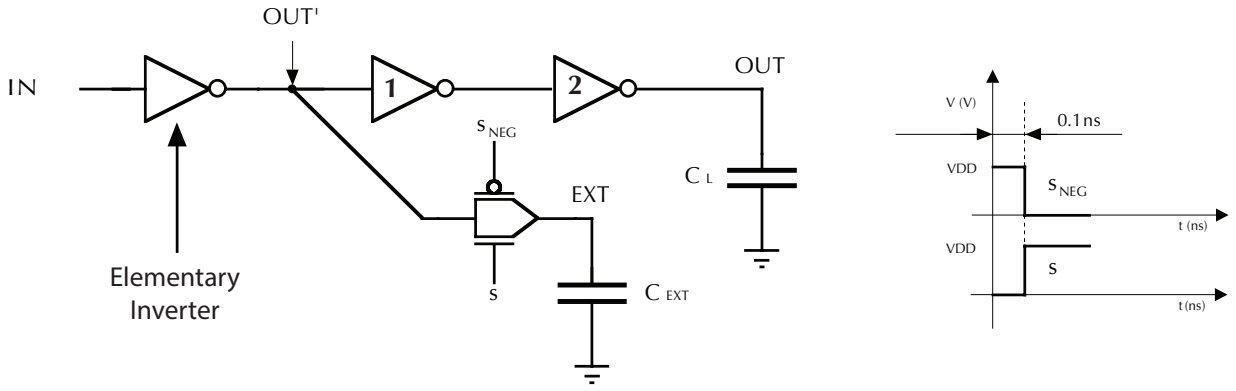

Figure 3