Exercise Circ16

Consider a CMOS fabrication process with the following parameters:

$k_n' = \mu_n C_{ox} = 90\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 30\ \mu A/V^2$,

$V_{th,n} = |V_{th,p}| = 0.6$ V,

$L_{min} = 0.5$ μm (minimjum allowed chanel length),

$t_{ox} = 16.5$ nm (gate oxide thickness),

$C_{ox} = 2.1$ fF/μm^2 (gate oxide capacitance per unit area),

$C_{ja} = 0.18$ fF/μm^2 (junction capacitance per unit area),

$C_{jsw} = 0.12$ fF/μm (junction capacitance per unit perimeter)
(the values of junction capacitance per unit area and per unit perimeter are averaged over the voltage swing from 0 V to VDD and are assumed equal for N^+- and P^+-regions).

$C_{metal1\text{-}substrate} = 0.05$ fF/μm^2 (metal-to-substrate capacitance per unit area – average value),

$C_{poly\text{-}substrate} = 0.06$ fF/μm^2 (polysilicon-to-substrate capacitance per unit area in field oxide regions),

$R_{\square metal1} = 2.1$ fF/μm^2 (sheet resistance of metal 1),

Consider now the elementary inverter shown in Figure 1, where we have the following values:

$W_N = 2$ μm (channel width for N-channel transistors);

$W_P = 6$ μm (channel width for P-channel transistors);

$L_N = L_P = L_{min}$ (channel length for N-channel and P-channel transistors);

A = 1.2 μm, B = 1.5 μm (in case other design rules, not specifically shown, are required to solve the exercise, they can be derived from the layout in Figure 1, assuming a layout grid with a pitch of 0.1 μm).

Supply voltage $V_{DD} - V_{SS}$ is equal to 3 V.

Lateral diffusion in MOS transistors, gate overlap (and fringing) capacitances, as well as any parasitic element non referred to above, can be assumed to be negligible.

The elementary inverter in Figure 1 is the basic element in a digital processing chain of an integrated circuit fabricated with the considered technology. The output capacitance to be driven by this processing chain is $C_L = 50$ pF.

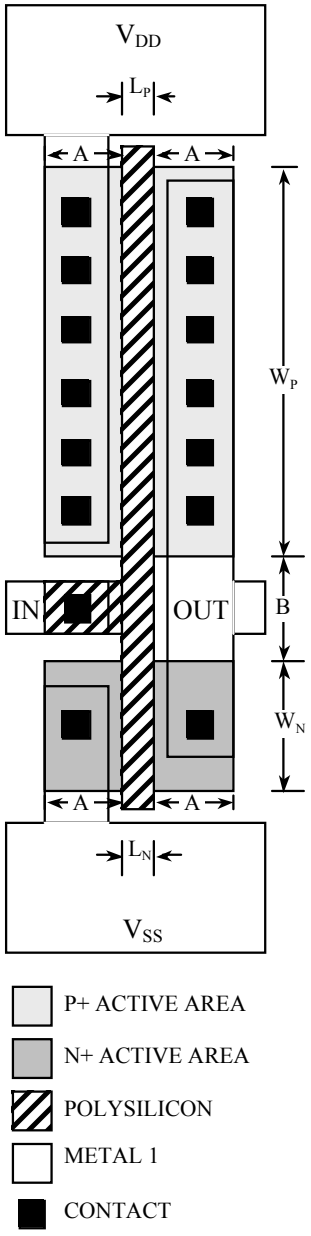

Figure 1

The candidate is asked to:

a) design a buffer to be placed between the last inverter of the processing chain and the capacitive load C_L having the minimization of the overall delay time as a target;
b) calculate the delay time from a transition of the input signal IN of the last inverter of the processing chain and the output signal OUT at the top plate of the load capacitor CL.