Exercise Circ17

Consider a CMOS fabrication process with the following process parameters:
$k_n' = \mu_n C_{ox} = 200\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 80\ \mu A/V^2$,
$V_{th,n} = |V_{th,p}| = 0.6$ V,
$L_{min} = 0.25\ \mu m$ (minimum allowed channel length, for both N-channel and P-channel transistors),
$C_{ox} = 3$ fF/μm^2 (gate oxide capacitance per unit area),
$C_{ov} = 0.10$ fF/μm (gate overlap capacitance per unit length per each side, including both overlap and fringing effects),
$t_{ox} = 10$ nm (gate oxide thickness).

Supply voltage V_{DD} is equal to 3 V.

The transistors in the elementary inverter used in an integrated circuit fabricated with the above process have the following sizes:

n-channel transistor: W_n (channel width) = 1 μm; L_n (channel length) = 0.25 μm;
p-channel transistor: W_p (channel width) = 2.5 μm; L_p (channel length) = 0.25 μm.

The used fabrication technology and the layout are such that, for each transistor, the drain capacitance and the source capacitance turn out to be equal to 40% and 40%, respectively, of the gate capacitance, whereas the capacitances associated to interconnections are negligible.

Consider the cirucit in Fig. 1, each inverter is equal to above elementary inverter.

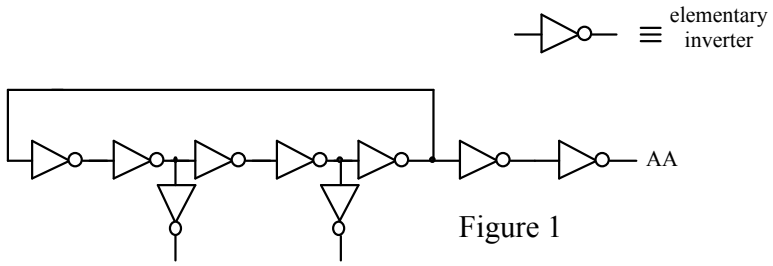

Figure 1

The candidate is asked to:

a) calculate the frequency of the waveform present at node AA (justifying all the assumptions made, if any);
b) calculate the frequency of the waveform present at node AA of a circuit obtained from the circuit in Fig. 1 by replacing the elementary inverter with an inverter whose transistors have the following sizes: W_n (channel width of N-channel transistor) = 2 μm; W_p (channel width of P-channel transistor) = 5 μm; L_n (channel length of N-channel transistor) = L_{min}; L_p (channel length of P-channel transistor) = L_{min};

Consider now, again, the circuit in its original version (i.e. the circuit where the transistors of the elementary inverter have the sizes con $W_N = 1$ mm; $W_P = 2.5$ mm; $L_N = L_P = L_{min}$). In order to drive en external load capacitance CL = 10 pF with no polarity inversion, two cascaded inverters (inv1 and inv2) are placed between node AA and the load (node OUT), as shown in Fig. 2. The candidate is now asked to:

c) design inverters inv1 and inv2 so as to minimize the delay time between node XX and OUT;
d) calculate the delay time between node XX and OUT;
e) provide considerations regarding the voltage waveform at node OUT.

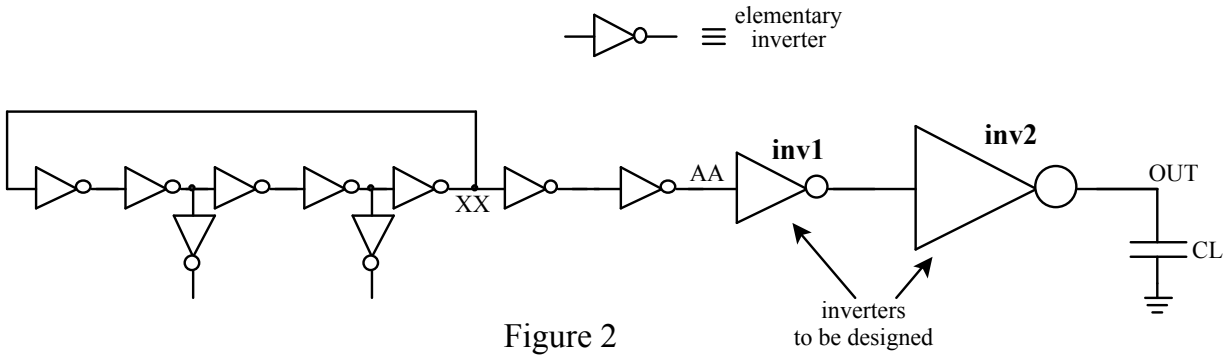

Figure 2