Exercise Circ19

Consider a CMOS fabrication process with the following process parameters:

$k_n' = \mu_n C_{ox} = 90\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 30\ \mu A/V^2$,

$V_{th,n} = |V_{th,p}| = 0.6$ V,

$W_{min} = 1.0\ \mu m$ (minimum allowed channel width for both N-channel and P-channel transistors),

$L_{min} = 0.5\ \mu m$ (minimum allowed channel length for both N-channel and P-channel transistors),

$C_{ox} = 2.2$ fF/μm^2 (gate capacitance per unit area),

$t_{ox} = 17$ nm (gate oxide thickness).

Supply voltage V_{DD} is equal to 3 V.

The candidate is asked to design an inverter able to ensure a delay time equal to 0.5 ns in the presence of an overall output capacitive load of 1.5 pF (in nominal conditions) in response to an ideal step-wise input.