Exercise Circ22

Consider a CMOS fabrication process with the following process parameters:

$k_n' = \mu_n C_{ox} = 80\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 60\ \mu A/V^2$,
$V_{th,n} = |V_{th,p}| = 0.6$ V,
$L_{min} = 0.35\ \mu m$ (minimum allowed channel length, for both N-channel and P-channel transistors),
$C_{ox} = 2.5\ fF/\mu m^2$ (gate oxide capacitance per unit area),
$t_{ox} = 12$ nm (gate oxide thickness).

Drain and source capacitances, as well as gate overlap capacitances, of each transistor can be assumed to be neglibile. Interconnection capacitances can also be assumed to be negligible.

Supply voltage V_{DD} is equal to 3 V.

Consider the circuit in Fig. 1. The sizes of the transistors used NAND and NOR gates are the following:

NAND gates:	*n*-channel transistor:	W_n (channel width) = 3.5 μm;	L_n (channel length) = 0.35 μm;
	p-channel transistor:	W_n (channel width) = 3.5 μm;	L_n (channel length) = 0.35 μm;
NOR gates:	*n*-channel transistor:	W_n (channel width) = 3.5 μm;	L_n (channel length) = 0.35 μm;
	p-channel transistor:	W_n (channel width) = 3.5 μm;	L_n (channel length) = 0.35 μm;

The candidate is asked to:

a) calculate the delay time of each gate in the circuit of Fig.1, justifying all the assumption made, if any;
b) estimate the oscillation frequency of the circuit in Fig. 1;
c) consider now the circuit in Fig. 2, where a NOR gate (identical to the other NOR gates used in the circuit) has been added to the circuit in Fig. 1 to drive an external capacitor C_L = 3 pF; the candidate is asked to calculate the rise and the fall time ot the voltage at node OUT and provide comments.

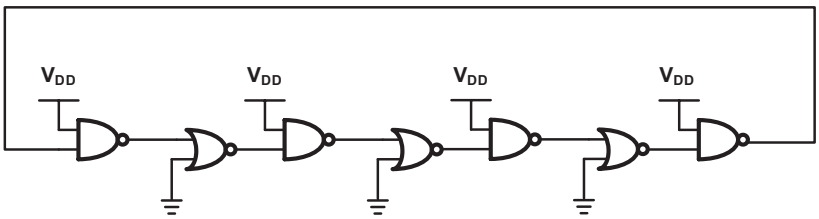

Figure 1

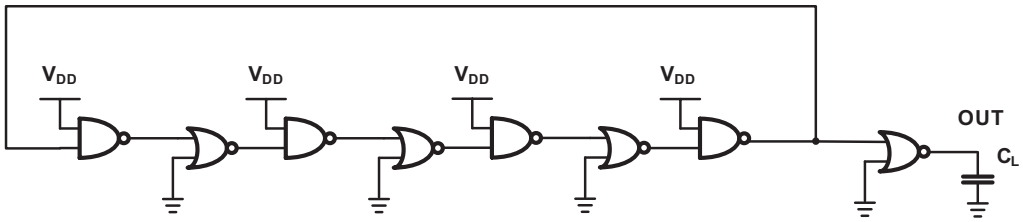

Figure 2

***NOTE**: The effects of the finite rise and fall time of input signal on the delay time of each gate may be assumed to be negligible throughout the whole exercise.*