Exercise Circ23

Consider a CMOS fabrication process with the following parameters:

$k_n' = \mu_n C_{ox} = 150\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 50\ \mu A/V^2$,

$V_{th,n} = |V_{th,p}| = 0.5$ V,

$L_{min} = 0.5$ μm (minimjum allowed chanel length),

$t_{ox} = 10$ nm (gate oxide thickness),

$C_{ox} = 3\ fF/\mu m^2$ (gate oxide capacitance per unit area),

$C_{ov} = 0.30$ fF/μm (gate overlap capacitance per unit length per each side, including both overlap and fringing effects).

Consider now an elementary inverter, where we have the following values:

$W_N = 2$ μm (channel width for N-channel transistor);

$W_P = 6$ μm (channel width for P-channel transistor);

$L_N = L_P = L_{min}$ (channel length for N-channel and P-channel transistors).

Supply voltage V_{DD} is equal to 3 V.

The used fabrication technology and the layout are such that, for each transistor, the drain capacitance and the source capacitance turn out to be equal to 20% and 20%, respectively, of the total gate capacitance, whereas the capacitances associated to interconnections are negligible.

Lateral diffusion in MOS transistors, as well as any parasitic element non referred to above, can be assumed to be negligible.

A buffer has to be included between the above elementary inverter and a load capacitor C_L equal to 5 pF.

The candidate is asked to:

a) design the buffer so as to substantially minimize the overall delay time from a transition of the signal, IN, applied to the input of the elementary inveter and the ensuing transition of the output signal, OUT;

b) calculate the delay time from a transition of input signal IN and the ensuing transition of output signal OUT when the buffer as designed from item a) is used;

Assume now that a series inductance L = 1.5 nH is present between the source terminal of the pull-down transistor of the buffer designed as from item a) and ground (V_{SS}), as shown in Fig. 4.

c) the candidate is asked to estimate the inductive noise that arises at the source terminal of the pull-down transistor of the last stage of the buffer designed at point a) due to a transition 1/0 of output signal OUT, which takes place as a consequence of the corresponding transition of input signal IN.

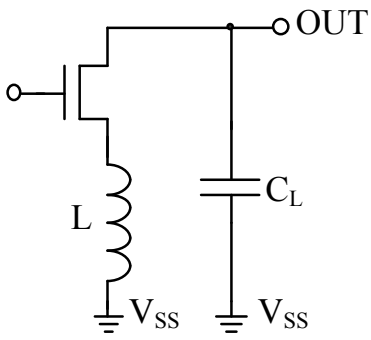

Figure 1