Exercise Circ24

Consider a CMOS fabrication process with the following process parameters:

$k_n' = \mu_n C_{ox} = 150\ \mu A/V^2$, $k_p' = \mu_p C_{ox} = 75\ \mu A/V^2$,
$V_{th,n} = |V_{th,p}| = 0.55$ V,
$L_{min} = 0.5\ \mu m$ (minimum allowed channel length, for both N-channel and P-channel transistors),
$C_{ox} = 2.5$ fF/μm^2 (gate oxide capacitance per unit area),
$C_{ov} = 0.20$ fF/μm (gate overlap capacitance per unit length per each side, including both overlap and fringing effects),
$t_{ox} = 12$ nm (gate oxide thickness).

Consider an elementary inverter whose transistors have the following sizes:

n-channel transistor: W_n (channel width) = 2 μm; L_n (channel length) = L_{min};
p-channel transistor: W_p (channel width) = 4 μm; L_p (channel length) = L_{min}.

The used fabrication technology and the layout are such that, for each transistor, the drain capacitance and the source capacitance are equal to 20% and 25%, respectively, of the overall gate capacitance, whereas the capacitances associated to interconnections are negligible.

Supply voltage V_{DD} is equal to 3 V.

The cascade of two suitably designed inverters has to be included, as a buffer, between the above elementary inverter and a load capacitor CL equal to 10 pF, as shown in Fig. 1.

The candidate is asked to:

a) design the two inverters 1 and 2 so as to adequately limit the overall delay time from a transition of input signal IN and the ensuing transition of output signal OUT;
b) calculate the delay time from a transition of input signal IN and the ensuing transition of output signal OUT when the buffer as designed form item a) is used;
c) assume now that a series inductance L = 2 nH and a series resistance R = 2 Ω are present between the source terminal of the pull-down transistor (M_D) of the last stage of the buffer designed as from item a) and ground (as shown in Fig. 2); the candidate is asked to estimate the noise that arises at the source terminal of transistor M_D due to a transition 1/0 of output signal OUT, which takes place as a consequence of a transition 0/1 of input signal IN in Fig. 1.

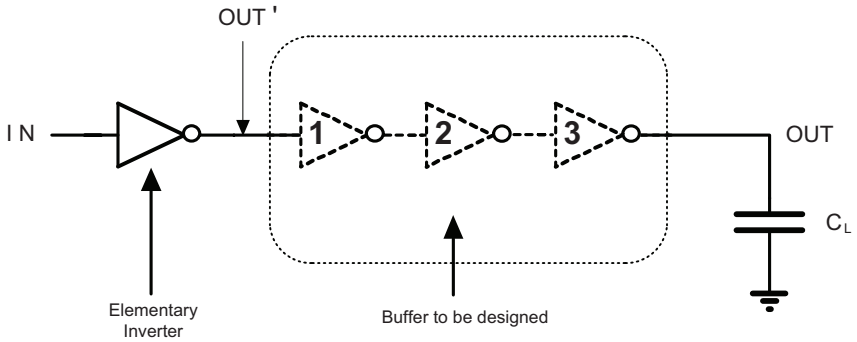

Figura 1

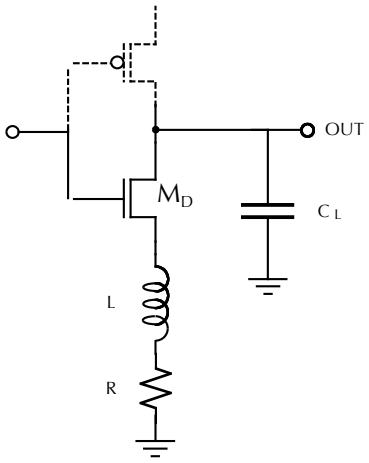

Figura 2