Exercise Log02

Consider the circuit in Figure 1, which has been designed by using logic cells and bocks belonging to the cell library illustrated in Table I. The circuit in Figure 3 is a part of a synchronous digital network. All input and output bits pass through positive edge triggered delay flip-flops (PETDFFs) controlled by clock signal Ck. Clock signal Ck, which is common to all PETDFFs, is not drawn in Figure 1 for simplicity. In Figure 1, PETDFFs are labelled as "FF" for simplicity.

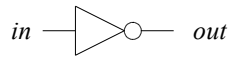
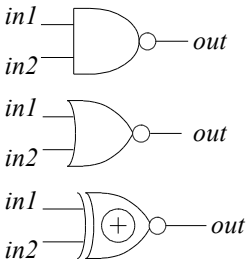
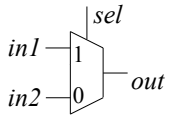
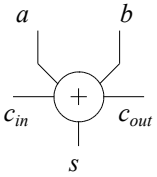
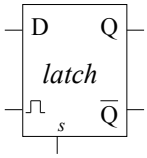
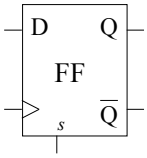
The candidate is asked to:

1. calculate the maximum allowed clock frequency for correct operation of the circuit (calculation details should be provided);
2. modify the circuit (by using only digital gates and circuit blocks of the considered library), so that the modified circuit can operate correctly at a frequency which is at least twice the frequency of the original circuit as calculated in the above point; check that the above design target is achieved.

The figure in the last page can be used for item 2.

Table I

The following table shows the (standard) cells available in the considered CMOS library, together with their timing characteristics.

Cell name	**Symbol**	**Parameter**	
Inverter		t_d = 0.4 ns	Delay time from input (*in*) to output (*out)*
NAND, NOR, XNOR (Inverting EXOR)		t_d = 0.7 ns	Delay time any from input (*in1, in2*) to output (*out*) (NAND and NOR gates with two or three inputs; inverting EXOR gate with two inputs)
Multiplexer		$t_{in,out}$ = 0.6 ns	Delay time from any input (*in1, in2*) to output (*out*)
		$t_{sel,out}$ = 0.55 ns	Delay time from select signal (*sel*) to output (*out*)
1-bit Full Adder (non inverting outputs)		t_s = 1.7 ns	Delay time from any input (*a*, *b*, c_{in}) to sum output (*s*)
		t_{cout} = 1.5 ns	Delay time from any input (*a*, *b*, c_{in}) to carry output (c_{out})
Positive level-sensitive latch with asynchronous SET (without asynchronous RESET)		$t_{d,q}$ = 1 ns	Delay time from input (*D*) to output, both non-inverting (*Q*) and inverting ($\overline{Q}$)
		$t_{ck,q}$ = 0.8 ns	Delay time from clock input transition 0/1 to output, both non-inverting (*Q*) and inverting ($\overline{Q}$)
		t_{su} = 0.45 ns	Set-up time
		t_h = 0.35 ns	Hold time
		t_s = 0.5 ns	Delay time from SET input (*s*) to output, both non-inverting (*Q*) and inverting ($\overline{Q}$)
		$t_{ck/2,min}$ = 1 ns	Minimum time duration of clock half-cycle (for both the high and the low level)
Positive edge triggered delay flip-flop (PETDFF) with asynchronous SET (without asynchronous RESET)		$t_{ck,q}$ = 0.8 ns	Delay time from clock input transition 0/1 to output, both non-inverting (*Q*) and inverting ($\overline{Q}$)
		t_{su} = 0.45 ns	Set-up time
		t_h = 0.35 ns	Hold time
		t_s = 0.5 ns	Delay time from SET input (*s*) to output, both non-inverting (*Q*) and inverting ($\overline{Q}$)
		$t_{ck/2,min}$ = 1 ns	Minimum time duration of clock half-cycle (for both the high and the low level)

For the sake of simplicity, we assume that the delay time of combinational gates is independent of the gate fan-in and the capacitive load.

For memory cells, SET signal (*s*) is assumed to be active high; in the case of PETDFF, the SET signal acts on both the master and the slave section.

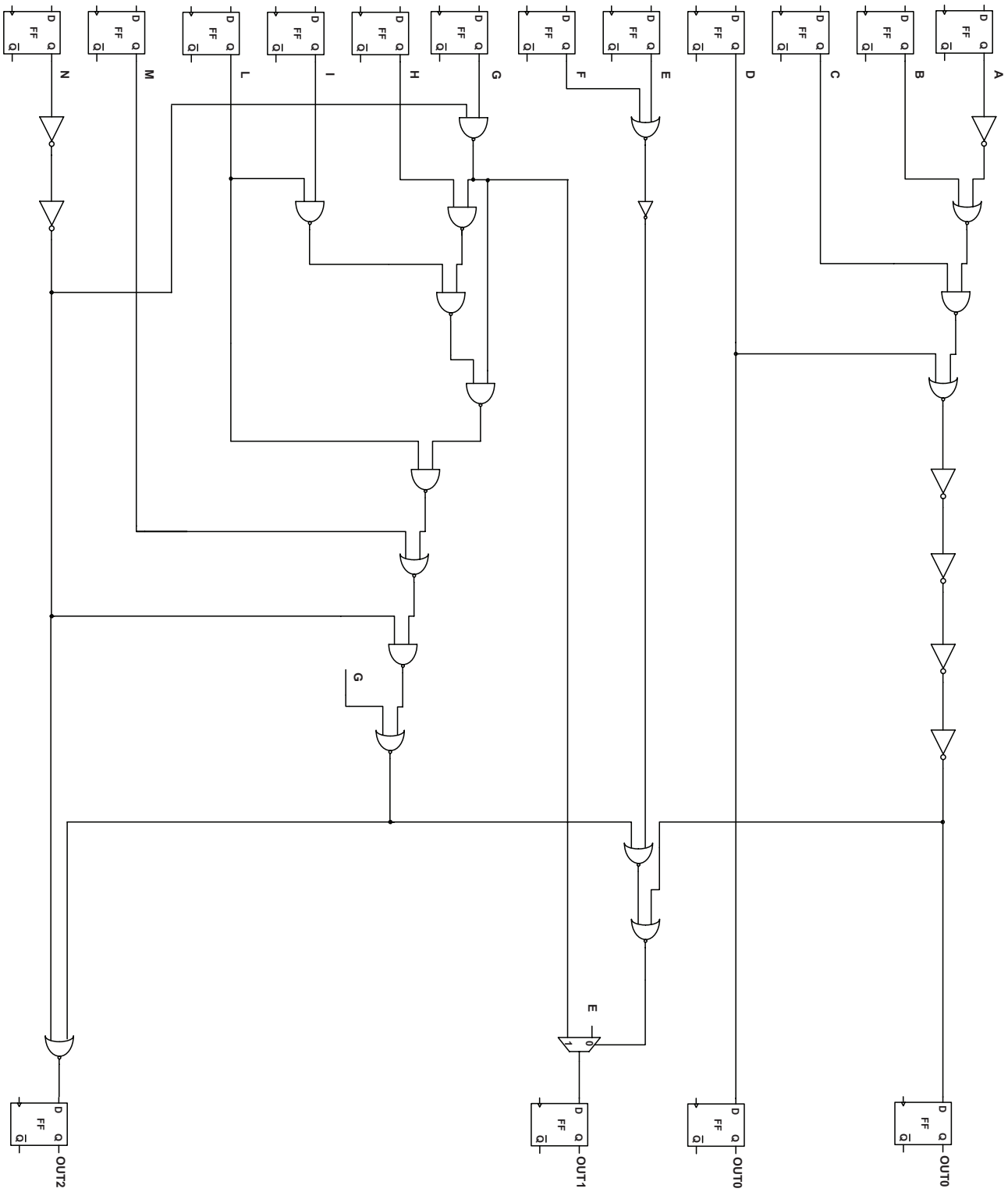
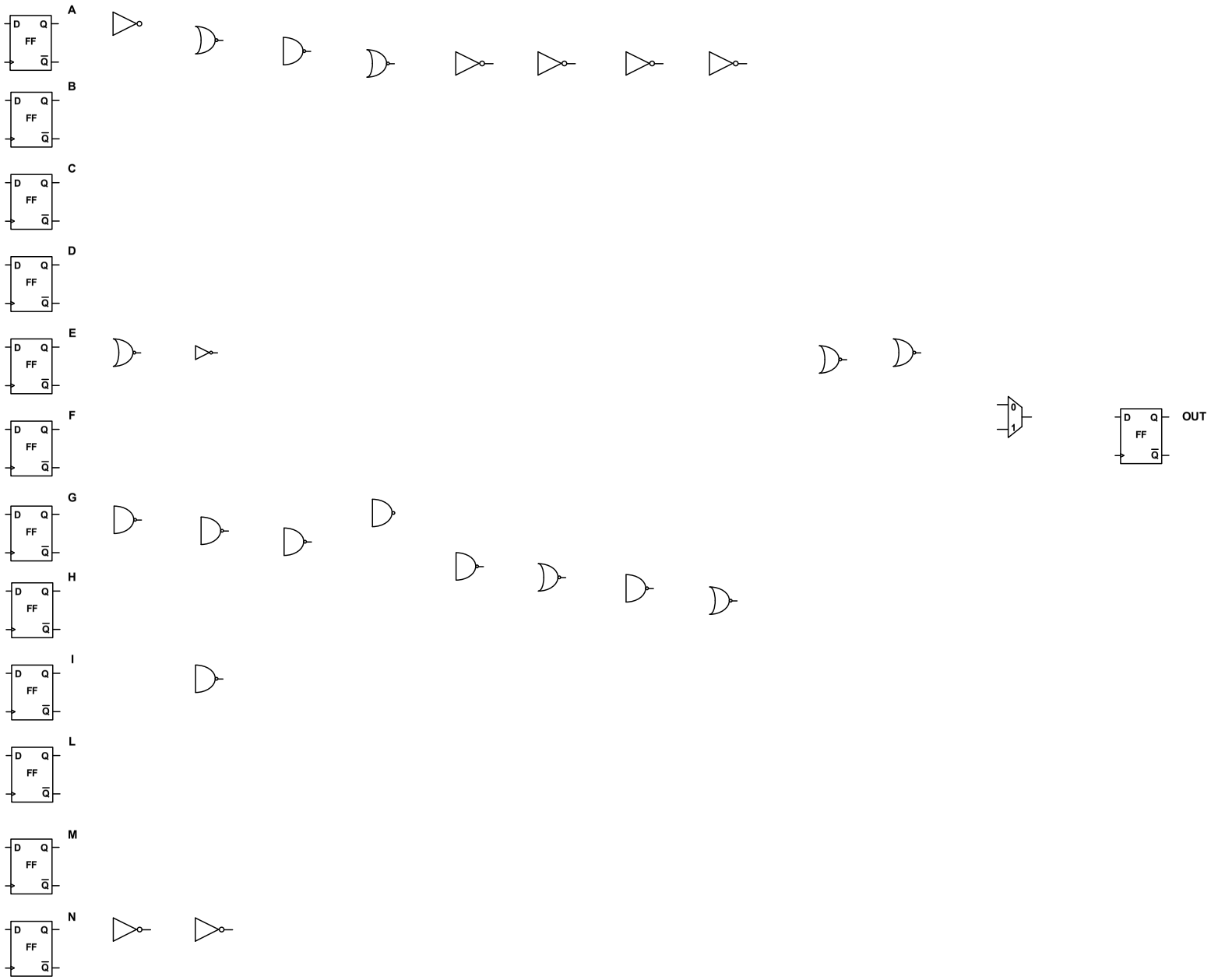


Figure 1


A
B
C
D
E
F
G
H
I
L
M
N
D
Q
FF
Q
0
1
OUT