Exercise Tim01

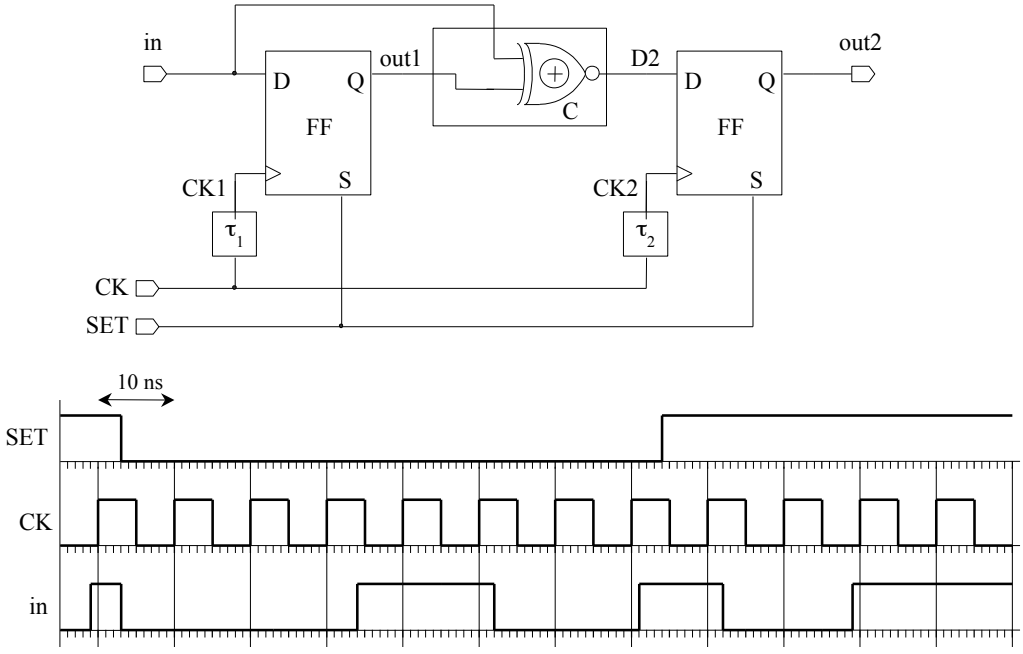
Consider the sequential network shown in the figure, where the circuit block labeled as "FF" for simplicity is a Positive Edge Triggered Delay Flip-Flop (PETDFF). The gates and the logic blocks have the following timing parameters:

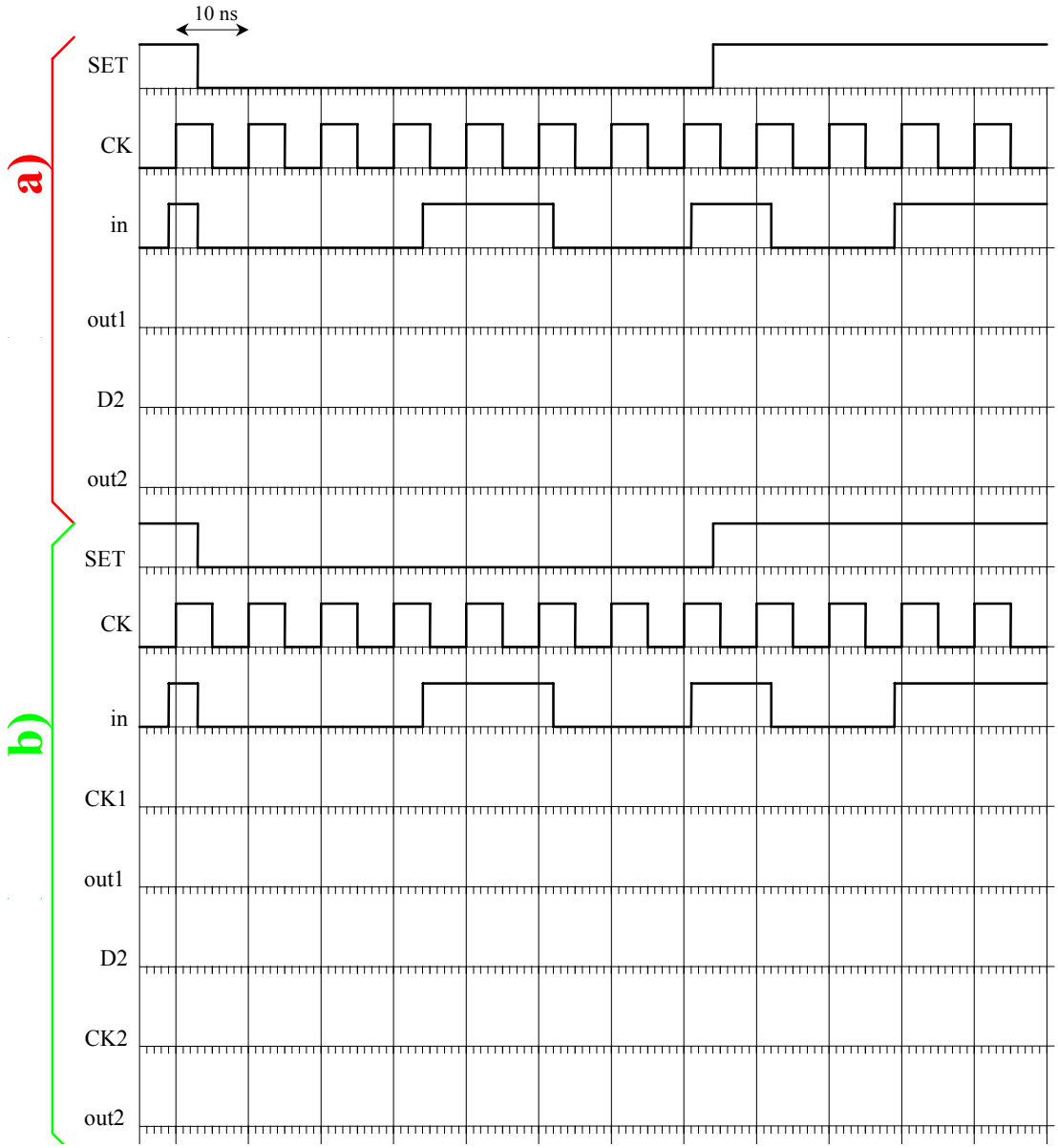
inverter delay time	: $t_{d,inv}$ = 0.5 ns;
EXNOR gate delay time	: $t_{d,EXNOR}$ = 1 ns
delay time from 0/1 transition of clock input to outputs Q, $\bar{Q}$ of PETDFFs	: $t_{ck,q}$ = 1 ns
delay time from 0/1 transition of asynchronous SET (S) input to outputs Q, $\bar{Q}$ of PETDFFs	: $t_{set,out}$= 1 ns
set-up time of PETDFFs	: t_{su} = 0.2 ns
hold time of PETDFFs	: t_h = 0.1 ns
minimum value of clock half-period $T_{CK}/2$ for the PETDFFs	: $T_{CK/2,min}$ = 2 ns

Note: RESET is assumed to be active when it is at a high level.

The waveforms of set (SET), clock (CK), and input (in) signals are given in the figure. The period of the clock signal, T_{CK}, is 10 ns. SET signal is assumed to be at a high level since at least 10 ns before the first clock period drawn in the figure.

The candidate is asked:
- to plot waveforms at nodes OUT1, D2, and OUT2 when $\tau_1 = \tau_2 = 0$ ns;
- to plot waveforms at nodes OUT1, D2, and OUT2 when $\tau_1 = 0$ ns, $\tau_2 = 5$ ns.




10 ns
a)
SET
CK
in
out1
D2
out2
b)
SET
CK
in
CK1
out1
D2
CK2
out2