Exercise Tim02

Consider the sequential network shown in figure 1, where the circuit block labeled as "FF" for simplicity is a Positive Edge Triggered Delay Flip-Flop (PETDFF). The gates and the logic blocks have the following timing parameters:

inverter delay time	: $t_{d,inv}$ = 0.5 ns;
EXNOR gate delay time	: $t_{d,EXNOR}$ = 1 ns
delay time from 0/1 transition of clock input to outputs Q, $\bar{Q}$ of PETDFFs	: $t_{ck,q}$ = 2 ns
delay time from 0/1 transition of asynchronous SET (s) input to outputs Q, $\bar{Q}$ of PETDFFs	: $t_{set,out}$= 1 ns
delay time from 0/1 transition of asynchronous RESET (r) input to outputs Q, $\bar{Q}$ of PETDFFs	: $t_{reset,out}$= 1 ns
set-up time of PETDFFs	: t_{su} = 0.2 ns
hold time of PETDFFs	: t_h = 0.2 ns
minimum value of clock half-period $T_{CK}/2$ for the PETDFFs	: $T_{CK/2,min}$ = 2 ns

Note: SET and RESET signals are assumed to be active when they are at a high level.

The waveforms of set, reset, and clock (ck) signals are given in figure2. The period of the clock signal, T_{CK}, is 10 ns. SET and RESET signals are assumed to be at a high and a low level, respectively, since at least 10 ns before the first clock period drawn in the figure.

The candidate is asked:
- to plot waveforms at nodes out1, D2, and out2 when τ = 0 ns;
- to plot waveforms at nodes out1, D2, and out2 when τ = 4 ns.

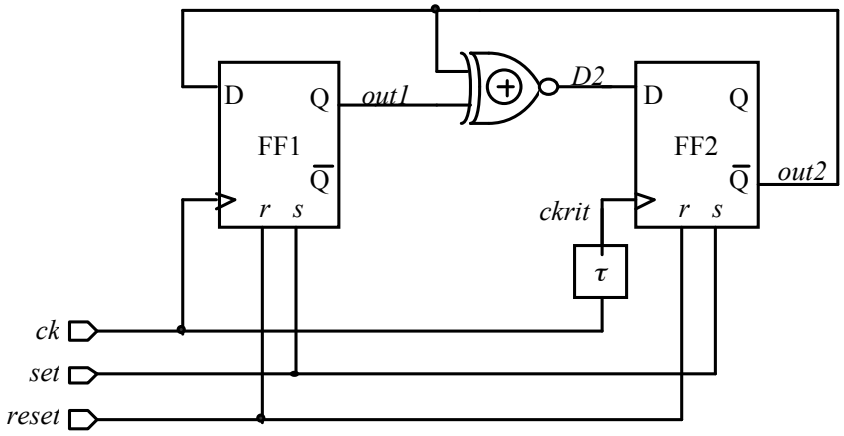

Fig. 1

NOTE
In the solution, red spikes show the presence of possible glitches at the output of the EXNOR gate due to the non simultaneous transition at the two inputs of this gate (it is not necessary to show these glitches in the solution of this exercise, since this has not been explicitly requested).

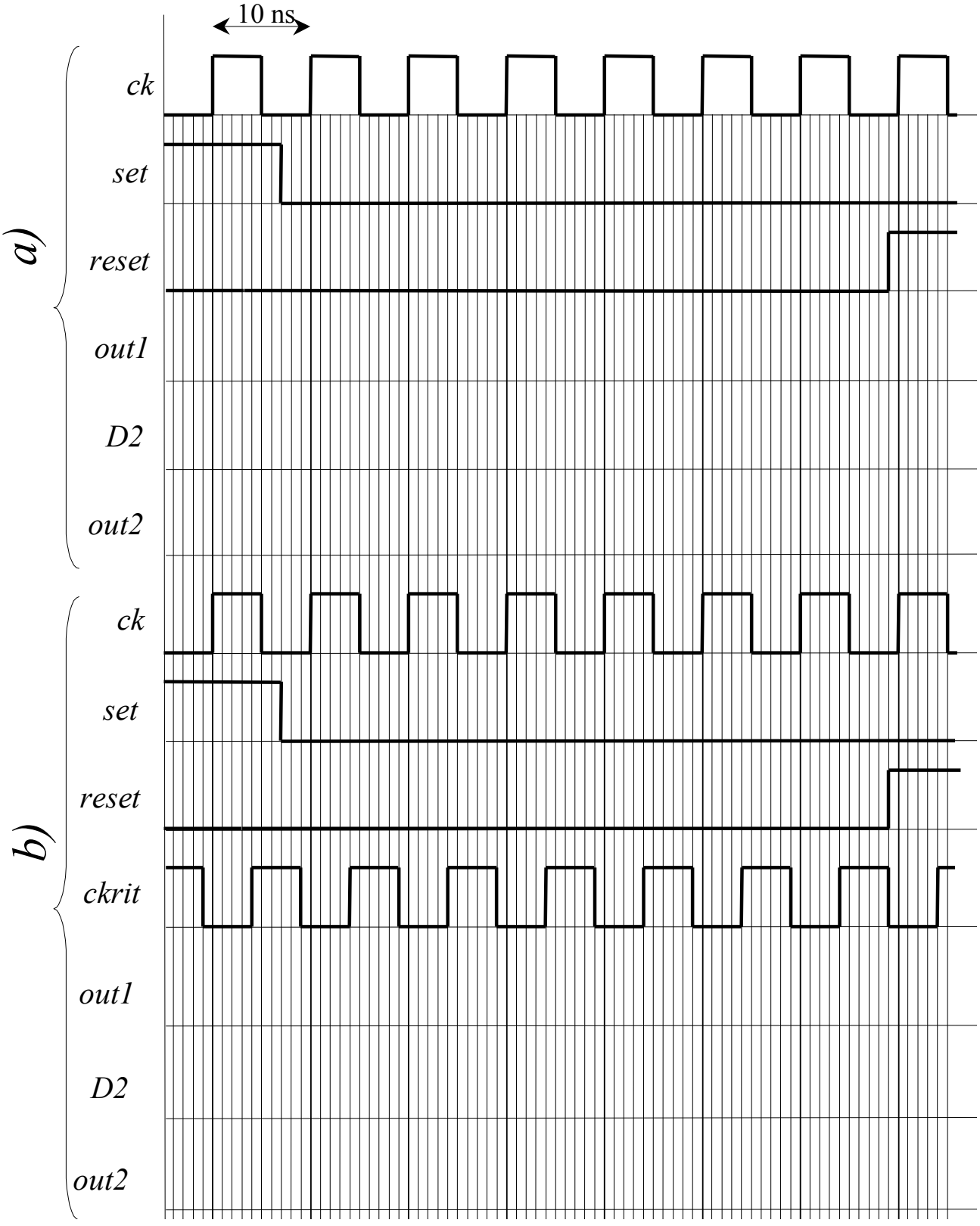
10 ns
a)
ck
set
reset
out1
D2
out2
b)
ck
set
reset
ckrit
out1
D2
out2

Fig. 2