A Common-Base Linear RF Power Amplifier for 3G Cellular Applications

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Abstract— A linear power amplifier for 3G cellular applications is presented. The amplifier operates in common-base configuration and can sustain output voltages in excess of $BV_{CEO}$. The chip, implemented in a 0.25μm SiGe:C technology, occupies 2.76 mm$^2$. When operated from a 4.5 V supply, the amplifier has a measured power gain of 20 dB at 1.85 GHz. At 1dB Compression Point, the amplifier delivers 27 dBm with a power-added efficiency of 33%. Saturated output power is 28.2 dBm with 37% power-added efficiency.

I. INTRODUCTION

Third-generation cellular [1] and modern wireless LAN standards use modulation schemes with high spectral efficiency but non-constant envelope and therefore require linear amplification. The high peak-to-average power ratio typical of these signals forces the power amplifier (PA) to work several dBs below its peak output power, even when transmitting at maximum average output power. As a result, for a given average output power, the optimum load impedance and the amplifier average efficiency are significantly reduced compared to constant envelope operation. This problem is even more difficult to address using the most advanced silicon processes. In fact, the tremendous improvements in $f_T$ and $f_{MAX}$ of modern SiGe and SiGe:C technologies have been partly achieved exploiting the tradeoff between transit time and breakdown voltage: i.e. higher $f_T$ and $f_{MAX}$ have been exchanged for a reduction in breakdown voltage [2][3]. The consequent reduction in supply voltage pushes the optimum load impedance further down. As the load impedance level is reduced, the impedance transformation ratio from the PA output to the antenna 50Ω load increases, making the matching network more sensitive to components variations and parasitic elements that ultimately impact operative bandwidth and efficiency. To address these issues, a common-base topology that is able to sustain output voltages well in excess of the collector-emitter breakdown voltage ($BV_{CEO}$) has been adopted in this work. The circuit topology and its voltage capability are discussed in Section II. Design and experimental results are reported in Section III. Section IV draws some conclusion.

This work has been carried out in the framework of the Italian National Research Program FIRB (contract nr. RBAP06LASS5).

II. COMMON-BASE POWER AMPLIFIER OPERATION

The classical solution adopted in the power stage of linear power amplifiers [4] is a common-emitter amplifier such as the one reported in Fig. 1. The optimum load is given by a parallel inductance that cancels out the total output capacitance seen at the transistor collector and a parallel resistance that is set essentially by the supply voltage and the desired power level:

$$R_{opt} = \frac{(V_{CC} - V_{SAT})^2}{2P_{SAT}}$$

where $V_{CC}$ is the supply voltage, $V_{SAT}$ is the minimum collector-emitter voltage that keeps the device in the linear operating region and $P_{SAT}$ is the maximum output power. An high supply voltage is desirable since it allows to deliver a large output power with a relatively high optimum load impedance, simplifying the output impedance transformation network. High speed SiGe technologies can sustain higher voltages compared to CMOS and are therefore usually preferred in RF power amplifier designs. As the technology evolves toward higher frequency capabilities, the contextual decrease in breakdown voltage pushes the supply voltage down, significantly lowering the optimum load impedance. At the technological level this has been addressed by providing several transistor designs, optimized for high power or high frequency operation [3]. Hence, using high-voltage transistors biased well below $BV_{CEO}$ is a viable, albeit inefficient, solution under optimum load conditions.
Fig. 2 Alternative PA configurations: a) cascode amplifier; b) cascode amplifier with inter-stage impedance-transformation network.

Nonetheless, ensuring reliable operation of a power amplifier in real-world conditions is less straightforward. In fact, load mismatch conditions, e.g. due to antenna impedance variations, can lead to instantaneous overvoltages that, for a voltage standing-wave ratio (VSWR) of 10:1, can go up to four times the supply voltage [5]. Under worst-case conditions, such as during battery recharge, an output voltage as high as 20 V may be reached [5]. This means that, even using high-voltage devices, special protection countermeasures need to be taken to avoid device failure. A possible solution comes from the device bias configuration. When the output voltage exceeds $BV_{CEO}$, avalanche current multiplication occurs in the collector-base junction and an additional current in the base terminal is generated, with opposite sign compared to the base bias current [3][6]. An avalanche current as small as the base bias current could then lead to device breakdown. On the other hand, if the bias network presents a sufficiently low impedance at the base terminal and has sufficient compliance to absorb the avalanche-generated current, the collector is allowed to rise significantly above $BV_{CEO}$ before reaching a breakdown condition, ideally up to collector-base breakdown ($BV_{CBO}$), which is much larger than $BV_{CEO}$. In order to approach this theoretical limit, the base impedance must be kept low at DC and all (even and odd) harmonics of the RF signal frequency. In practice, achieving this condition without introducing undue losses in the RF path is not trivial in a common-emitter amplifier, where the input RF signal and the bias network are connected through the same terminal (i.e. the base) to the power transistor. The most straightforward and reliable solution would be to use a cascode amplifier, as shown in Fig. 2.a. This solution makes it easy to provide a low impedance at the base terminal of the output (common-base) transistor, where no RF signal is present, by simply using a large capacitor, while the common-emitter device is protected from high voltages by the common-base device. On the other end, such a configuration is highly inefficient because the voltage stacking of the two devices, both working at high current levels, significantly increases power dissipation. A more efficient solution, conceptually similar to the one proposed in [7], is shown in Fig. 2.b. The inter-stage passive impedance transformation network scales down the impedance level going from the common-emitter to the common-base device. This amounts to a passive current amplification and, as a result, the common-emitter device signal current level is significantly lower compared to the common-base device. Assuming that the inter-stage network is AC-coupled, the common-emitter device can be biased at a reduced current level, in principle proportionally to the current amplification contributed by the inter-stage network. A simplified version of the circuit implementation proposed in this work is reported in Fig. 3. The circuit consists of a power stage ($Q_2$), a driver stage ($Q_1$) and an inter-stage LC matching network. The power stage provides voltage and power amplification and has nominally unity current gain. Hence, its power gain is given by the ratio of the load and input (emitter) impedance. The LC resonator formed by $L_D$ and $C_D$ resonates at the fundamental frequency and, together with $Q_2$, provides current amplification. In fact, ignoring the parasitic capacitance at the output of the driver, the RF signal current flowing in $L_D$ and $C_D$ (hence also in $Q_2$) is equal to the driver’s output current multiplied by the loaded quality factor ($Q$), given by

$$Q = \left( \frac{1}{Q_D} + \frac{C_D}{L_D g_{m2}} \right)^{-1} = \frac{L_D}{Q_D g_{m2}}$$

(2)

where $g_{m2}$ is the transconductance of the power transistor and $Q_D$ is the quality factor of inductor $L_D$. The use of an LC network to perform the current amplification allows for a certain degree of flexibility in the choice of the current gain, the upper bound to the gain being the inductor
quality factor. A large capacitance $C_D$, hence a low inductance $L_D$, is desirable in order to minimize the contribution of the inductor quality factor $Q_D$ to the loaded $Q$ and the relative weight of the driver output capacitance compared with $C_D$, minimizing the sensitivity to parasitic elements. In this way most of the power supplied by the driver stage is delivered to the power stage and the loaded $Q$ is less dependent on process variations. On the other hand, as $C_D$ is increased, current gain decreases. The choice of $C_D$ also impact the driver efficiency. From this point of view, $C_D$ should be set according to the optimum loading condition:

$$Q_D \frac{L_D}{C_D} = R_{opt,DRF} \equiv \frac{(V_{CC1} - V_{SAT})}{I_{RF}}$$

III. CIRCUIT DESIGN AND EXPERIMENTAL RESULTS

The complete schematic of the common-base power amplifier is shown in Fig. 4. The PA was designed in a low cost 0.25μm SiGe:C technology from ST-Microelectronics. The technology features high breakdown voltage transistors with $BV_{CEO}$ of 6 V and $BV_{CEO}$ of 19 V, typical $f_T$ equal to 30 GHz and $f_{MAX}$ of 60 GHz. A differential solution was chosen to further boost the optimum impedance load. In fact, using a differential topology, the optimum (differential) load is increased by a factor of four compared to the expression in (1). The PA was optimized to operate according to 3GPP/UMTS specifications [1] in power class 3, with a center frequency of 1.95 GHz, average output power of 24 dBm and peak output power around 27 dBm. The voltage supply for the power stage was set to 4.5 V, to ensure safe operation even in the worst load mismatch conditions and avoid thermal runaway [8]. Estimating a $V_{SAT}$ of about 1V, with a supply voltage $V_{CC}$ set to 4.5 V, the optimum differential load resistance is approximately 50 Ω or 25 Ω per side. In practice, due to parasitic elements and non-linearity, a lower impedance is required, or equivalently an higher signal current. The power stage transistors were designed in order to reach the desired power level with maximum efficiency and linearity. In fact when the output impedance is fixed, there is only one transistor size (in terms of total emitter area and device unit size) which maximizes linearity and efficiency for the desired output power. If the transistor is made larger than the optimum size voltage compression will dominate the output power compression; if the transistor’s size is lower than the optimum, current compression dominates [1]. The transistor optimum size has been found by sweeping the transistor size with fixed optimum load and by simulating the output power and efficiency. At the power stage’s output, a common-mode series resonant network is used to shunt second harmonic components in the output current in order extend the linear output range. Since second harmonics appear as a common mode, only one common-mode small-sized .

![Fig. 4 Complete circuit schematic of the differential common-base power amplifier with the driver stage.](image)

![Fig. 5 Die microphotograph](image)
An inductor ($L_A$ in Fig. 4) is needed, saving area. The series capacitance is made controllable using MOS switches, allowing to accommodate for process variations. A bond-wire is used to supply the DC current at the power stage emitter. This bond-wire does not carry RF signal current and, due to the low impedance present at the emitter, the exact value of its inductance is not important as long as it is sufficiently high. The driver stage provides additional stable power gain and supplies the necessary current drive to the power stage. The inter-stage matching network was sized to obtain a current gain of about 4. According to the inductor model and circuit simulations the loss due to the finite inductor $Q$ is less than 1 dB. Since the power level is much lower than in the power stage, a cascode amplifier can be used in the driver stage, improving reverse isolation and with limited impact on the overall efficiency. The driver was designed such that power compression occurs at a power level greater than the maximum input power needed by the output stage. The overall power compression is then dominated by the power stage. The chip microphotograph is reported in Fig. 5. The die area is 2.76 mm$^2$. The chip was tested in a chip-on-board configuration. Three bond-wires are used for each output: one connected to the power supply and two connected to the signal output. A 4 pF capacitor toward ground on each output implements a close-to-optimum impedance transformation. Optimum loading was achieved using manual impedance tuners, whose outputs are measured using a dual-input power meter. The tuners are individually adjusted to compensate for the inevitable mismatch in bond-wire inductances when using non-automated bonding techniques. The measured tuner loss (0.2 dB), cable and connectors loss (0.3 dB) are de-embedded from the measurements. Precise input impedance matching was not implemented, hence exact power gain measurements were not possible. The measured power gain, output power and power-added-efficiency at 1.8 GHz are shown in Fig. 6. The measured 1dB compression point, saturated output power and related efficiencies as a function of frequency are shown in Fig. 7.

**IV. CONCLUSIONS**

Linear power amplifier design issues associated with the lowering breakdown voltages in advanced SiGe processes are addressed in this work. A common-base linear power amplifier which can sustain output voltages in excess of $BV_{CEO}$ is presented. The chip, implemented in a 0.25μm SiGe:C technology, when operated from a 4.5 V supply, has a measured power gain of 20 dB at 1.85 GHz. At 1dB Compression Point, the amplifier delivers 27 dBm with a power-added efficiency of 33%. Saturated output power is 28.2 dBm with 37% power-added efficiency.

**ACKNOWLEDGMENT**

The authors gratefully acknowledge A. Liscidini and F. Ramaioli for help with testing. The authors wish to thank K. Torki (CMP) for design kit support.

**REFERENCES**


**Fig. 6** Measured power gain, output power and PAE at 1.8 GHz.

**Fig. 7** Measured P-1dB and power added efficiency versus frequency.