On the Design of Single-Inductor Multiple-Output DC-DC Buck Converters

Massimiliano Belloni, Edoardo Bonizzoni, and Franco Maloberti
Department of Electronics
University of Pavia
Via Ferrata, 1 – 27100 Pavia – ITALY
[massimiliano.belloni, edoardo.bonizzoni, franco.maloberti]@unipv.it

Abstract – Design techniques for single inductor multiple output (SIMO) DC-DC buck converters are presented. The suitable control of a multiple feedback loop enables the sharing of a single inductor with many outputs with a good stability and limited cross regulation. The method has been verified with simulations at the behavioural and transistor level to obtain four independent regulated output voltages ranging from 0 V to 1 V below the power supply voltage. The use of a suitable analog processing of errors allows obtaining a power efficiency as high as 86%.

I. INTRODUCTION

The fast market growth of battery-operated portable applications such as digital cameras, personal digital assistants, cellular phones, MP3 players, medical diagnosis systems, etc. demands for more and more efficient power management systems. In this area, DC-DC converters play a critical role in keeping long battery life while still providing stable supply voltage together with the required driving capability [1]. In these devices, an inductor stores magnetic energy and transfers part of it to a load while another part is converted into electrostatic energy stored in a capacitor. The result is high power efficiency, low cost, and small size [2], [3]. Often, in portable applications, the reduction of power is obtained by using multiple supply voltages for different functional blocks [4]. A dynamic regulation of the supply following the performance requests optimizes the use of power. However, since having in the system one inductor per DC-DC converters is expensive and not practical, the strategy is viable only if two or more converters share the same inductor as proposed in recent implementations (single inductor multiple output boost converter [5] and boost or buck converters with double output [6], [7]). Since the regulation of each output requires its loop control, a multiple-output system must foresee a multi-feedback loop with the request of suitable processing of signals. Moreover, it is necessary to use extra power switches that must be properly driven.

This paper studies the above mentioned design problems and applies the identified solutions to a study case: a four-output single inductor buck converter able to independently regulate the output voltages in the range 0 V - 1 V below the power supply voltage and able of an overall driving capability of 0.8 A. The switching frequency is 3 MHz and the external inductor is 1 μ H.

Transistor level simulations show that a power efficiency as high as 86% can be achieved.

II. SIMO ARCHITECTURE

A DC-DC converter with multiple outputs time-shares the inductor current among different loads. Fig. 1 shows a buck converter with N -outputs. While a normal buck has just a PWM control for the high-side and low-side switches (namely MP and MN), the N -output buck uses N additional power switches (SW_i , $i = 1, \dots, N$) for the time-sharing of the inductor current. The switches can be n -channel (with possible boost), p -channel or complementary devices. The choice depends on a trade-off between complexity and cost (area, power efficiency and so forth).

The control subsystem, together with the drivers, provides N control signals. One is used to obtain the buck converter switching, and the others to divide the clock period into N slots.

The processor foresees N control loops with as inputs the errors of the N outputs, $\epsilon_i = V_{set,i} - V_{out,i}$. The buck converter operates in the continuous mode, but the current, I_i , delivered to the $C_{out,i}$ output capacitor, is discontinuous, since it goes to zero when the corresponding switch opens, as shown in Fig. 2 for $i = 1, \dots, 4$. During the discontinuous period the current of the load is provided by the capacitance $C_{out,i}$.

Figure 1. Block diagram of the N -output SIMO buck converter.

Figure 2. 4-output SIMO inductor (I_L) and output branches currents (I_i).

Fig. 2 shows an example of inductor and load switched currents for four outputs. The diagrams of the figure support the definition of the main duty cycle D and the sharing duty cycles. They can be expressed, respectively, as

$$D = \frac{T_{on,MP}}{T} \quad (1)$$

$$D_i = \frac{T_{on,SW_i}}{T} \quad (2)$$

where $T_{on,MP}$, T , and T_{on,SW_i} are the on-time of the p -channel switch MP , the clock period, and the on-time of the i -th n -channel output switch SW_i , respectively.

III. SINGLE-INDUCTOR DUAL-OUTPUT CONTROL EQUATIONS

In order to study the control strategy let us consider before a single-inductor dual-output (SIDO) DC-DC buck converter, as shown in Fig. 3. The figure also depicts the load currents in the cases $D < D_1$ and $D > D_1$.

If the ripple of the output voltages is small, the derivative of the inductance current in the three time-slots identified by the duty cycles D and D_1 ($D_1 + D_2 = 1$) can be assumed constant. Therefore, in the steady state we have

$$(V_{dd} - V_{out,1})D = V_{out,1}D_1 + V_{out,2}D_2; \text{ for } D < D_1 \quad (3)$$

$$(V_{dd} - V_{out,1})D_1 + (V_{dd} - V_{out,2})D_2 = V_{out,2}D_2; \text{ for } D > D_1 \quad (4)$$

that, after rearranging, both become

$$V_{dd}D = V_{out,2} + (V_{out,1} - V_{out,2})D_1 \quad (5)$$

Assuming that the inductor current ripple is negligible, its average value $\bar{I}_L$ can be used to determine the output currents

Figure 3. 2-output SIMO and output branches currents (I_i) in the two cases $D < D_1$ and $D > D_1$.

$$\bar{I}_L D_1 = \bar{I}_{out,1} = \frac{V_{out,1}}{R_{load,1}} \quad (6)$$

$$\bar{I}_L (1 - D_1) = \bar{I}_{out,2} = \frac{V_{out,2}}{R_{load,2}}$$

that gives

$$D_1 = \frac{R_{load,2} V_{out,1}}{R_{load,2} V_{out,1} + R_{load,1} V_{out,2}} \quad (7)$$

Equation (7) together with (5) makes a system to control D and D_1 . Unfortunately, the control is difficult to implement using the errors because it involves nonlinear terms and needs the estimation of the load currents. However, from (5) it can be noted that the main duty cycle is proportional to the weighed sum of the output voltages. With $D_1 = 1/2$, (5) becomes

$$D = \frac{V_{out,1} + V_{out,2}}{2V_{dd}} \quad (8)$$

that suggests to control the main duty cycle using the sum of the errors $\epsilon_1 = (V_{set,1} - V_{out,1})$ and $\epsilon_2 = (V_{set,2} - V_{out,2})$. Indeed, the optimum control should account for the value of D_1 . However, the use of the plain sum of errors, instead of their dynamic weighted sum, is an affordable (and reasonable) approximation.

By differentiating equation (7), it is possible to obtain

$$\delta D_1 = \alpha \cdot \epsilon_1 - \beta \cdot \epsilon_2 \quad (9)$$

where α and β are coefficients that depend on the output voltages and the load resistances. Therefore, the control loop controlling D_1 should use the weighted subtraction of errors. An approximated solution is to use the plain subtraction of errors. The two above strategies for the control of D and D_1 are intuitively justified. In fact, positive errors call for more energy to be delivered to the loads and this is obtained by increasing D (see Fig. 4). A positive ϵ_1 or a negative ϵ_2 indicates the need to increase the fraction of power delivered to load 1 and vice-versa.

The control method for two outputs can be extended to multiple outputs. The sum of errors should control the main duty cycle and proper combinations of errors control the sharing duty cycles. More in general, for an N -output DC-DC buck converter, N control variables $X_1, \dots, X_N$ can be defined.

Figure 4. Control of D and D_1 as required by errors ϵ_1 and ϵ_2 .

$$\begin{aligned}
X_1 &= a_{11}\varepsilon_1 + a_{12}\varepsilon_2 + \dots + a_{1N}\varepsilon_N \\
X_2 &= a_{21}\varepsilon_1 + a_{22}\varepsilon_2 + \dots + a_{2N}\varepsilon_N \\
&\dots \\
X_N &= a_{N1}\varepsilon_1 + a_{N2}\varepsilon_2 + \dots + a_{NN}\varepsilon_N
\end{aligned} \tag{9}$$

The gain of each control loop must tend to null each error combination in (9), thus leading to:

$$\begin{aligned}
a_{11}\varepsilon_1 + a_{12}\varepsilon_2 + \dots + a_{1N}\varepsilon_N &\rightarrow 0 \\
a_{21}\varepsilon_1 + a_{22}\varepsilon_2 + \dots + a_{2N}\varepsilon_N &\rightarrow 0 \\
&\dots \\
a_{N1}\varepsilon_1 + a_{N2}\varepsilon_2 + \dots + a_{NN}\varepsilon_N &\rightarrow 0
\end{aligned} \tag{10}$$

Indeed, equation (10) is an homogeneous system of N equations in the N unknowns ε_i . To have only one solution, the determinant of the system characteristic matrix must be

$$\det \begin{pmatrix} a_{11} & a_{12} & \dots & a_{1N} \\ a_{21} & a_{22} & \dots & a_{2N} \\ \dots & \dots & \dots & \dots \\ a_{N1} & a_{N2} & \dots & a_{NN} \end{pmatrix} \neq 0 \tag{11}$$

For 4 outputs, a simple form of the characteristic matrix and then the errors coefficients in (9) is

$$\begin{aligned}
X_1 &= \varepsilon_1 + \varepsilon_2 + \varepsilon_3 + \varepsilon_4 \\
X_2 &= \varepsilon_1 - \varepsilon_2 - \varepsilon_3 - \varepsilon_4 \\
X_3 &= \varepsilon_1 + \varepsilon_2 - \varepsilon_3 - \varepsilon_4 \\
X_4 &= \varepsilon_1 + \varepsilon_2 + \varepsilon_3 - \varepsilon_4
\end{aligned} \tag{12}$$

In order to ensure stability to the system, it is necessary to associate the control voltages X_i to proper control variables. In our case X_1 , X_2 , X_3 , and X_4 are related to the duties D , D_1 , $D_1 + D_2$, $D_1 + D_2 + D_3$, respectively.

Fig. 5 shows the conceptual scheme of the 4-output case control system together with the $PWMs$ output pulses. $H(s)$ in the main path is a first-order zero-pole filter that achieve the loop compensation, while A blocks in the sharing paths are just amplifiers. The main path, driven by $H(s)X_1$, controls the main switches MP and MN , while the other paths, driven by AX_2 , AX_3 , and AX_4 , manage the sharing of the inductor current, thus determining the four time-sharing slots.

Figure 5. Conceptual scheme of the analog processor and PWMs output pulses.

IV. DESIGN EXAMPLE

The above-described methods have been tested on a 4-output design, simulated at the behavioural, transistor level (with a 0.18- μm CMOS technology), redesigned and fabricated on silicon using a 0.5- μm 2-poly, 5-metals CMOS technology. A short description of that design and the experimental results is given in [8]. The target specifications of this design example are to have a total current up to 0.8 A, a switching frequency of 3 MHz with a single 1- μH inductor and 10- μF capacitors. The simulations at the behavioural level show an excellent matching with the expected results. Fig. 6 shows the inductor current (top) and its sharing among the four output branches (bottom). The inductor current ripple is in the range from 0.32 to 0.54 A and shows the change of slope due to the different regulated voltages. Other performance are also verified.

Figure 6. Simulink™ simulation result of the inductor current.

Figure 7. Detail of the main processing path.

After the behavioural simulations, which prove the system functionality, transistor level simulations provide additional verifications of the circuit operation. The technology used is a 0.18- μm CMOS technology with high voltage option. The signal processing required by (12) can be realized in the analog or the digital domain. In the latter case, it is necessary to have an on-board A/D converter as it is often done in modern buck converter.

For analog implementations, the use of switched-capacitor schemes is a convenient choice because they enable inverting and non-inverting functions. Fig. 7 shows the scheme for the main processing path. It consists of three blocks. The first section combines the errors and provides a gain; the second is the first order zero-pole switched-capacitor filter. C_5 and V_{bias} achieves a DC level shift. The third block is a flip around double

sample-and-hold necessary to decouple the filter from the *PWM*, thus limiting the kickback from the switching part and eliminating the glitches produced by the switching from phase 1 to phase 2. The other processing channels do not require filtering and are realized with only two sections. One is to process the errors, providing gain and shifting the DC level; the other is the sample-and-hold.

Fig. 8 shows the simulated output voltages V_{outi} regulated at 0.85 V, 1.5 V, 1.2 V, and 1.78 V, respectively. The power supply voltage is equal to 3.3 V. The output currents are $I_{out1} = 45$ mA, $I_{out2} = 350$ mA, $I_{out3} = 40$ mA, and $I_{out4} = 180$ mA, thus achieving a total delivered output current of 0.615 A. The simulated maximum output voltage ripple is about 25 mV (V_{out3}).

Figure 8. Simulated output voltages.

Fig. 9 shows the results of a cross-regulation test. V_{out4} is set to 1.8 V driving 300 mA to its load. V_{out1} and V_{out2} present a step-up variation from 1.2 to 1.7 V and from 0.8 to 1.6 V, respectively. I_{out1} and I_{out2} rise up from 150 to 212 mA and from 50 to 100 mA, respectively. V_{out3} has a step-down variation from 1.4 V to 0.9 V and its current decreases from 70 to 45 mA. The output voltage drop due to the cross-regulation is less than 24 mV.

Figure 9. Cross-regulation simulations.

Fig. 10 shows the simulation results of a load-regulation test with a supply voltage of 3.3 V. The four output voltages V_{outi} are set to 1.2 V, 1 V, 1.6 V, and 1.8 V, respectively. I_{out1} and I_{out3} have a step-up variation from 75 mA to 240 mA and from 150 mA to 250 mA, respectively, while I_{out2} and I_{out4} present a step-down variation from 200 mA to 100 mA and from 300 mA to

125 mA, respectively. The output voltage drops due to the load-regulation is less than 1.5% in all cases.

Several simulations have been performed in order to evaluate the system power efficiency performance. The simulated peak of power efficiency is 86%, considering a supply voltage of 3.3 V and an overall output current equal to 400 mA. With other conditions the efficiency is lower but within the entire range of specifications the power efficiency is always higher than 74%.

Figure 10. Load-regulation simulated results.

V. CONCLUSIONS

In this paper, the design methodologies for single-inductor multiple-output DC-DC buck converter have been presented. The new control method suitable for any number of outputs is more robust than 2-output counterparts. The approach has been verified for 4 outputs with behavioural simulations and transistor level verifications. With a 0.18- μ m CMOS technology, it is possible to achieve a 0.8 A driving capability with a peak of efficiency of 86%. The same design method has been used for a 0.5- μ m CMOS technology that experimentally verified the approach functionality, [8].

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