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A 200-mA, 93% peak power efficiency, single-inductor, dual-output DC–DC buck converter

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Abstract A single-inductor dual-output (SIDO) DC–DC buck converter is presented. The circuit uses only one (external) inductor to provide two independent output voltages ranging from 1.2 V to the power supply (2.6–5 V) with a maximum total output current of 200 mA. The proposed converter has been fabricated in a 0.35-μm p-substrate CMOS technology. Measurement results demonstrate that a peak power efficiency as high as 93.3% can be achieved. An automatic substrate bias switch technique, that cancels the body effect of the p-channel output power transistors, improves the converter power efficiency performance.

Keywords DC–DC converters · Buck converter · Single-inductor dual-output

1 Introduction

The fast market growth of battery-operated portable applications such as digital cameras, personal digital assistants, cellular phones, MP3 players, medical diagnosis systems, etc. demands for more and more efficient power management systems. In this area, DC-DC converters play a critical role in keeping long battery life, while still providing stable supply voltage together with the required driving capability [1]. In these devices, the most important but critical component is the inductor that stores magnetic energy and transfers part of it to a load while another part is converted into electrostatic energy in a capacitor and stored. Key features of DC–DC converters are high power efficiency, low cost, and small size. A DC–DC converter in buck configuration regulates a high input voltage into a lower one [2, 3]. Figure 1 shows a circuit diagram of a buck converter. The transistor M_1 operates at a frequency, with period T, and with an on-time to period ratio or duty-ratio $T_{ON}/T = d$. By considering all components ideal, the relationship between steady-state input (V_{in}) and output (V_{out}) voltages and duty-ratio turns out to be $V_{out} = dV_{in}$. Since the value of d lies between 0 and 1, the converter output voltage must be less than or equal to the input voltage.

Recently, in portable applications, a widely adopted strategy to reduce power consumption consists in using multiple supply voltages for different functional blocks [4]. In these cases, conventional implementations of DC–DC buck converters may consist of N independent converters, where N is the number of required output voltages. This solution leads to waste of components, and, hence, of area of the PCB where the system is mounted. Furthermore, this method will increase the overall cost of the system. The need for devices able to supply independent loads, while minimizing the number of external components is, hence, evident. In this respect, the single-inductor multiple-output (SIMO) approach seems to be very promising [5]. When designing a SIMO DC-DC converter two main issues have to be considered: the need of an inductor time sharing technique, in order to efficiently distribute the energy stored

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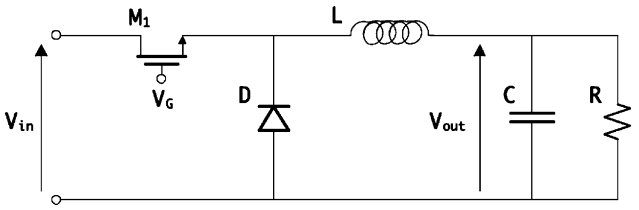

Fig. 1 DC–DC buck converter circuit diagram

in the inductor over the output branches and the need of power transistors on the load side together with an adequate driving strategy for these transistors. The latter point is less critical in the case of SIMO boost converter [6–8] design. Indeed, in these circuits, power switches are already present on the load side and, starting from output voltages always higher than the power supply value, it is relatively easy to obtain an adequate and efficient driving strategy for these output switches. By contrast, in the case of SIMO buck converters, additional power transistors are required on the load side. Moreover, considering that the output voltages are always lower than the power supply value, it is more challenging to provide a driving strategy for the output power transistors able to ensure adequately low on-resistance and, hence, high power efficiency performance.

In this paper, a single inductor dual output (SIDO) DC–DC buck converter is presented. The proposed circuit uses one (external) inductor to provide two independent output voltages ranging from 1.2 V to the power supply voltage V_{dd}, which in turn ranges from 2.6 to 5 V. The system overall driving capability is 200 mA and the switching frequency is 1 MHz. An automatic substrate bias switch technique that cancels the body effect of the p-channel output power transistors improves the converter power efficiency performance. The proposed SIDO buck converter has been fabricated in a 0.35-μm p-substrate CMOS technology. Measurement results demonstrate that a peak power efficiency as high as 93.3% can be achieved.

2 Chip architecture and power transistors

The basic idea behind any multiple output DC–DC buck converter is to share the magnetic energy stored in the single inductor between different independent loads. By using a dedicated control strategy, the current flowing through the inductor can be switched from one load to the other, according to the voltage setting and current values required from each output load.

In the particular case of two output loads, it can be noted that the inductor sustains a voltage proportional to the derivative of the current switching from one load working at a given voltage to another load at a different voltage. This causes a change of the slope of the inductor current,

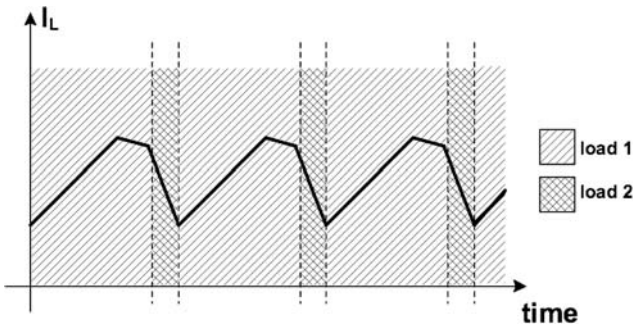

Fig. 2 Inductor current time diagram

I_L, leading, for example, to a time diagram like the one shown in Fig. 2. It is worth pointing out that the switching of the inductor from V_{dd} to ground can occur before or after the load switching. Moreover, the operation illustrated in Fig. 2 is for continuous operations and, in the shown case, the inductor changes to ground before loads are switched. Figure 3 shows the circuit diagram of the proposed single inductor dual output DC–DC buck converter. The inductor L is connected to the output branches by means of switches M_2 and M_3. Storage capacitors C_1 and C_2 act as filters for the two output voltages, V_{OUT1} and V_{OUT2}, respectively, while R_1 and R_2 represent the corresponding output loads. To correctly control the system, it is necessary to determine two switching control signals, one for the normal PWM operation and the other for the load switching. Therefore, the control circuit should use two feedback loops having the two output errors as input variables.

Many solutions can be used, but for systems that admit a ripple of the order of tens of millivolt, with switching frequencies of the order of 1 MHz and requiring a fast settling time response, the best trade-off is to use two conventional PWM loops driven by the two output voltage errors. The resulting pulses D_1 and D_2 are used for the two functions needed. The modulated signals are easily achieved by means of the error amplifiers A_1 and A_2 and of the voltage comparators CMP_1 and CMP_2, connected in cascade. Switches M_1 and M_4 are obviously realized with n-channel and p-channel devices, respectively. By contrast, the choice for implementing M_2 and M_3 is problematic. There are two possibilities: use a p-channel device or complementary devices. When one of the regulated voltages is much lower than the battery voltage, the driving voltage of the p-channel (equal to the regulated voltage) may not be sufficiently large and having an n-channel device whose $V_{GS} = V_{DD} - V_{OUT}$ could be helpful. However, the cost of this solution is too high in terms of silicon area. This design uses only a p-channel device. PMOS transistors M_1, M_2, and M_3 have a W/L ratio of 18000/0.6, while NMOS transistor M_4 is 6000/0.6. These aspect ratios arise from a trade-off between the on-resistance of the switches, the waste of

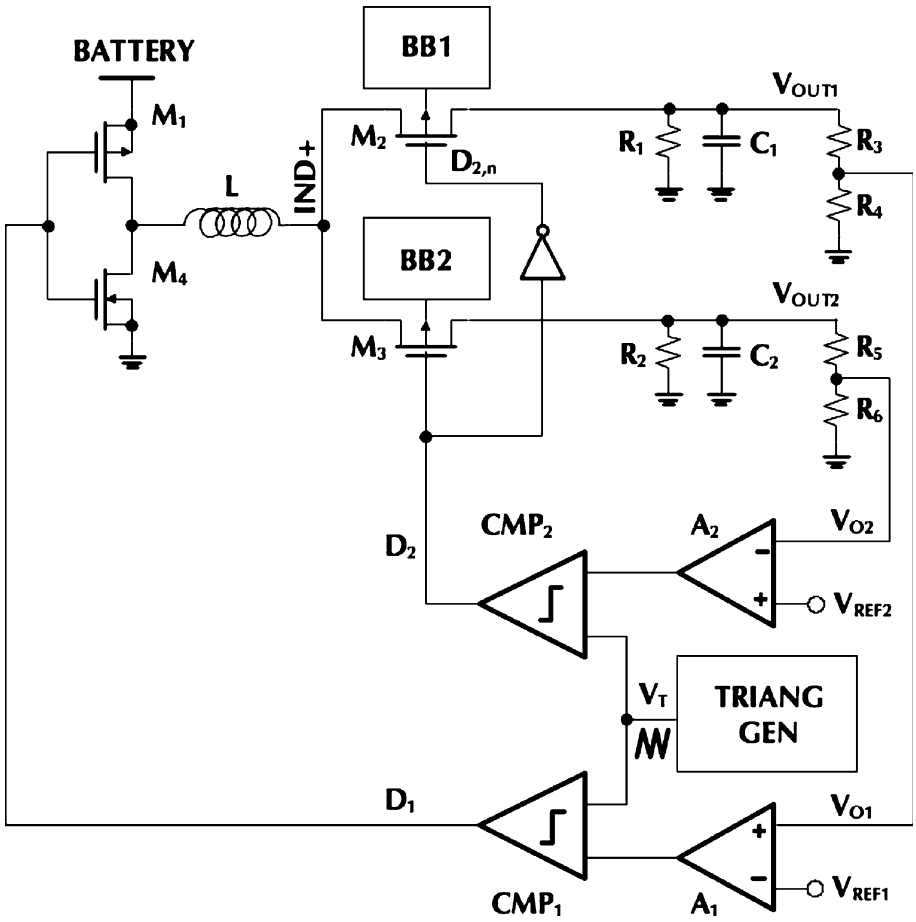

Fig. 3 SIDO circuital diagram

silicon area, and the dynamic power consumption. The used channel length (about twice the minimum) minimizes transistor leakage currents and ensures proper ESD protection. It is worth to point out that each 18000/0.6 PMOS transistor layout uses 360 fingers (50/0.6 each) arranged in 5 modules (72 fingers each). A V-shaped metal2-metal3 sandwich connection optimizes the current density distribution in the transistor.

It is known that the on-resistance of the p-channel switches depends on the aspect ratio and the threshold voltage, whose value, for transistors M_2 and M_3, changes because of the body effect. Notice that, depending on the technology and the operating condition, the value of the on-resistance can increase by 20%, worsening the efficiency for certain output current ranges. The optimum solution is to bias the p-channel substrates to the source voltage. However, when the switch is off, the source is the highest between the two regulated voltages. Therefore, the optimum substrate biasing would require to dynamically switch between the voltages across the transistor channel terminals. This function is ensured by circuits *BB1* and *BB2*, that dynamically bias the bulk terminals of transistors M_2 and M_3 to the highest voltage between the switching node *IND+* and the output voltages V_{OUT1} and V_{OUT2}, respectively. In this way, the body effect of the p-channel output power transistors is canceled during the on-phases, thus improving the converter power efficiency performance. During the off-phase, the bulk dynamic biasing avoids undesired bulk currents. Circuit details of blocks *BB1* and *BB2* are discussed in the next Section.

Notice that transistors M_2 and M_3 could be also implemented by using n-channel devices. This solution leads to a lower area occupancy, but requires to boost the gate voltages of M_2 and M_3 by means, for instance, of a charge pump [9]. The power consumption of the boost circuit affects the overall DC–DC converter power efficiency. Using n-channel and boosted control makes sense for low regulated voltages. In our design p-channel devices have been preferred to implement transistors M_2 and M_3, as the lowest output is 1.2 V.

3 Basic building blocks

The operational amplifier used as error amplifier is a simple mirrored single stage with an open loop gain of 35 dB and a gain-bandwidth product (f_T) equal to 30 MHz. The voltage comparators CMP_1 and CMP_2 consist of a

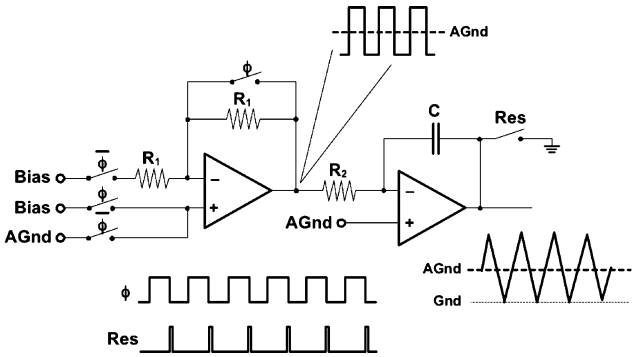

Fig. 4 Schematic diagram of the triangular waveform generator

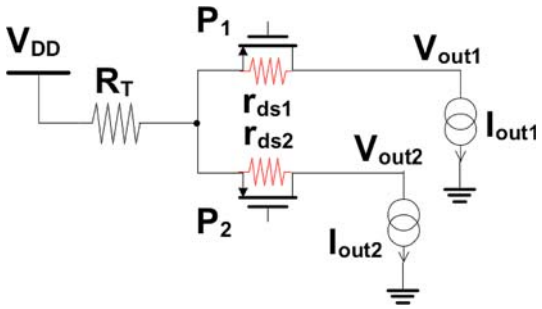

Fig. 6 SIDO simple model for the evaluation of the power efficiency (charging phase)

differential stage followed by a tapered inverter chain [10], as required in order to correctly drive the large capacitive gate terminals of transistors M_2 and M_3.

The control circuit is based on a triangular waveform, generated by the circuit (referred to as *TRIANG GEN* in Fig. 3) reported in Fig. 4. This control circuit leads to PWM switching and load switching at different times, so that it never occurs that the switches on the two sides of the inductor are both off. This ensures a better operation of the snubbers. In particular, as mentioned in the previous Section, two conventional PWM loops driven by the two output voltage errors control the system. The error on V_{OUT1} manages the current to be injected in the converter by acting on the battery side transistors. The error on V_{OUT2} controls how to distribute the current flowing through the inductor over the two output loads, according to the voltage setting and current values required from each output branch. Stability of the two control loops has been verified with long time domain simulations. A square wave signal whose analog ground level and amplitude are controlled by the *AGnd* (i.e., $V_{dd}/2$) and bias generator is integrated by the op-amp A_2 and R_2C. To make sure that offset or leakage currents do not shift the triangular waveform, a reset phase forces the output to analog ground at each clock cycle.

Figure 5 shows the schematic diagram of blocks *BB1* and *BB2*, used to dynamically bias the bulk terminal of M_2 to the highest voltage between *IND+* and V_{OUT1}. Two differential pairs amplify the differences between the regulated voltage and the *IND+* terminal of the inductor. A tapered chain of inverters controls the bias switching. Notice that a possible offset of the differential pair is not critical because problems arise when an incorrect substrate biasing is in the order of several tens of millivolt.

A simple behavioral model enables to evaluate and better investigate the improvement in the system power efficiency due to the automatic substrate bias switch technique. In Fig. 6, R_{DS1} and R_{DS2} represent the drain-to-source resistances of power transistors P_1 and P_2, respectively. Resistor R_T summarizes the resistive effects due to the on-resistances of the battery side power transistors (i.e., M_1 and M_4 of Fig. 3) and to the resistance of the coils of the external inductor. The system power efficiency in steady state (i.e., the power is calculated for periodic waveform) becomes

$$\eta = \frac{P_{L1} + P_{L2}}{P_{L1} + P_{L2} + P_0 + P_{diss1} + P_{diss2}} \quad (1)$$

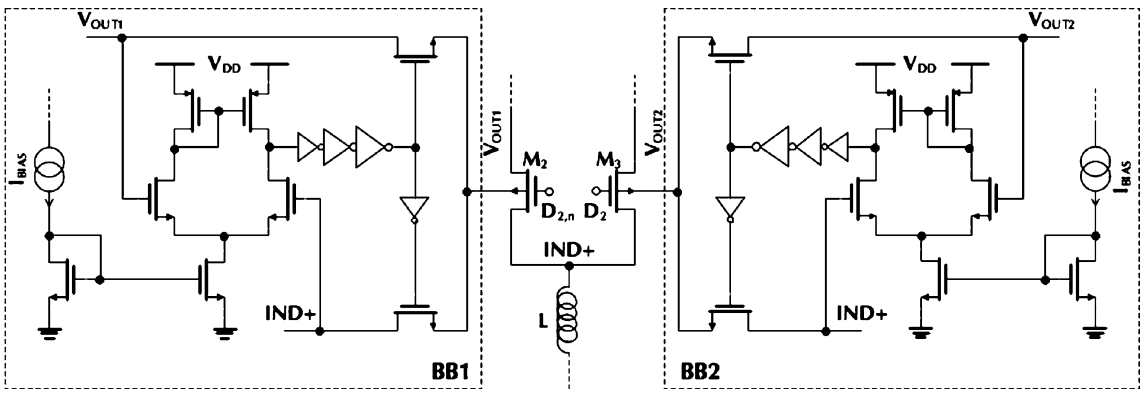

Fig. 5 Schematic diagram of the bulk biaser circuits

where $P_{L1} = {}^1\!/_T \int_0^T V_{\text{out1}}(t) \cdot I_{\text{out1}}(t)\mathrm{d}t$ and $P_{L2} = {}^1\!/_T \int_0^T V_{\text{out2}}(t) \cdot I_{\text{out2}}(t)\mathrm{d}t$ are the average output powers for the two loads and P_0 is the power lost in the battery side, whose expression is

$$P_0 = R_{\text{T}} \frac{1}{T} \int_0^T (I_{\text{out1}}(t) + I_{\text{out2}}(t))^2 \mathrm{d}t + P_{\text{dyn,0}} \tag{2}$$

and $P_{\text{dyn,0}}$ is the dynamic power consumption required to drive the power transistor gates of the battery side.

P_{diss1} and P_{diss2} in (1) can be respectively expressed as

$$P_{\text{diss 1}} = R_{\text{DS1}} \frac{1}{T} \int_0^T I_{\text{out1}}^2(t)\mathrm{d}t + P_{\text{dyn,1}} \tag{3}$$

$$P_{\text{diss 2}} = R_{\text{DS2}} \frac{1}{T} \int_0^T I_{\text{out2}}^2(t)\mathrm{d}t + P_{\text{dyn,2}} \tag{4}$$

where $P_{\text{dyn,1}}$ and $P_{\text{dyn,2}}$ are the dynamic power consumptions lost to drive the MOS transistors of the output branches. In (3) and (4), R_{DS1} and R_{DS2} are modeled by the fitting equations

$$R_{\text{DS1}} = \frac{1}{\mu_{\text{P}} C_{\text{OX}} \frac{W}{L} (V_{\text{out1}} - V_{\text{th1}}) - \alpha I_{\text{out1}}} \tag{5}$$

$$R_{\text{DS2}} = \frac{1}{\mu_{\text{P}} C_{\text{OX}} \frac{W}{L} (V_{\text{out2}} - V_{\text{th2}}) - \alpha I_{\text{out2}}} \tag{6}$$

respectively, where the parameter α accounts for the saturation of the electrical field for high currents [11]. The threshold voltage of a MOSFET is

$$|V_{\text{th}}| = |V_{\text{th,0}}| + \gamma \left\{ \sqrt{|V_{\text{SB}} - 2\Phi_{\text{FS}}|} - \sqrt{|2\Phi_{\text{FS}}|} \right\} \tag{7}$$

The model enables the estimation of the system power efficiency both with and without the body effect on the output power transistors. To be more specific, the first case considers the wells of the output power transistors connected to the supply voltage, while in the second case the output power transistors wells are always connected to their source terminal. The latter case corresponds to adopt an automatic substrate bias switch technique, as in the presented converter.

Figure 7 shows the simulated power efficiency of the system as a function of the first output current, by keeping the power supply set to 3.6 V and the output current on the second load equal to 40.2 mA. It can be noted that the bulk biaser circuits improve the power efficiency performance of about 4% for light loads. This improvement decreases to about 2.5% for medium–high loads.

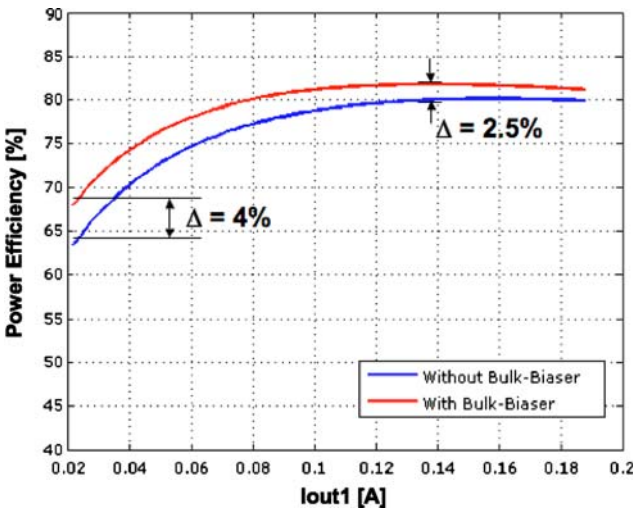

Fig. 7 Simulated power efficiency with and without bulk biaser circuits

4 Experimental results

The proposed single-inductor dual-output buck converter has been fabricated in a 0.35-μm, 5-V transistor option, p-substrate, 2-poly, 3-metal level CMOS technology. Figure 8 shows the chip microphotograph. The chip area is 1,350 μm × 1,800 μm, including pads. Figure 8 highlights the power transistor area, which is about 0.22 mm^2. In

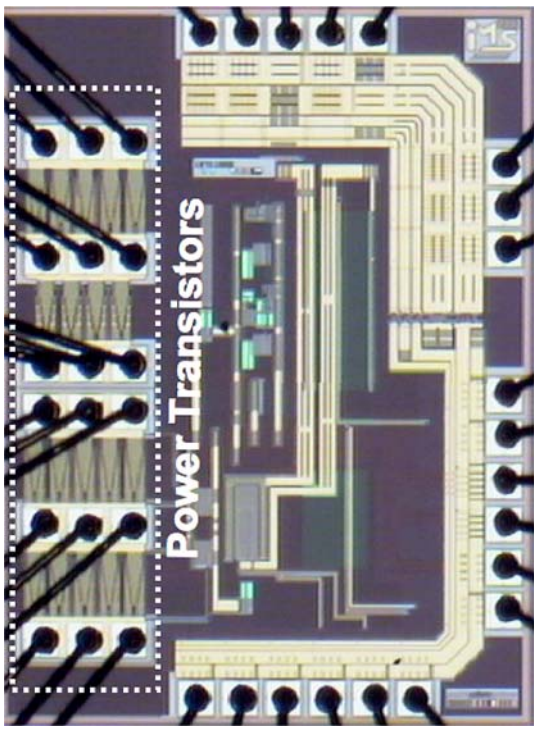

Fig. 8 Chip microphotograph

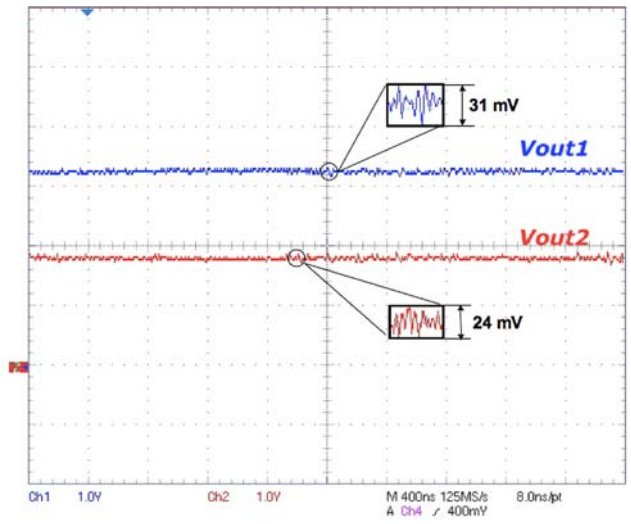

Fig. 9 Measured output voltages

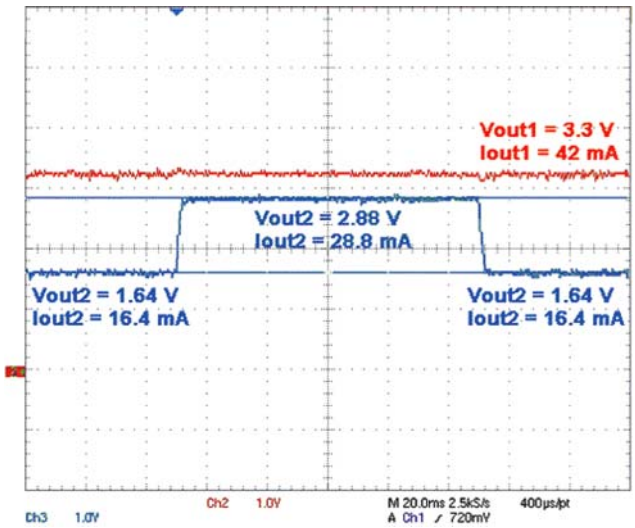

Fig. 11 Measured step response ($V_{OUT1} = 3.3$ V, $V_{OUT2} = 1.64$ V–2.88 V–1.64 V)

order to minimize the resistance and the inductance of the bonding wires, a triple bonding approach has been adopted for the drain and the source terminals of each power transistor. The used off-chip inductor and storage capacitors, referred to as L, C_1, and C_2, respectively, are 22 µH and 35 µF, respectively. The switching frequency is 1 MHz.

Figure 9 depicts the measured output voltages. The power supply value is equal to 3.6 V. Voltages V_{OUT1} and V_{OUT2} are set to 3.3 and 1.8 V, respectively. The achieved voltage ripple is 31 mV for V_{OUT1} and 24 mV for V_{OUT2}, with output currents of 56 and 40 mA, respectively.

Figure 10 shows the cross-regulation of the output voltages, with one output fixed at 3.3 V (V_{OUT1}) and the other (V_{OUT2}) changing by 680 mV, from 1.42 to 2.1 V. The increase of the current on the second load from 22 to 33 mA does not affect V_{OUT1} at all.

Again, Figure 11 depicts the cross-regulation of the output voltages, with one output fixed at 3.3 V (V_{OUT1}), delivering to its load 42 mA and the other (V_{OUT2}) changing by 1.24 V, from 1.64 V up to 2.88 V and again down to 1.64 V. As in the case reported in Fig. 10, it can be noted that the increase and the decrease of the current on the second load from 16.4 to 28.8 mA and from 28.8 to 16.4 mA does not affect V_{OUT1}.

Figure 12 shows the cross-regulation of the output voltages, with the second output V_{OUT2} set at 2.3 V delivering 21 mA to its load and the other (V_{OUT1})

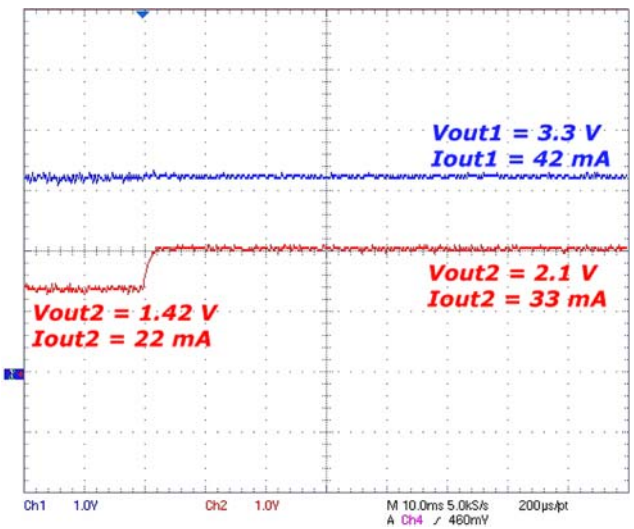

Fig. 10 Measured step response ($V_{OUT1} = 3.3$ V, $V_{OUT2} = 1.42$ V–2.1 V)

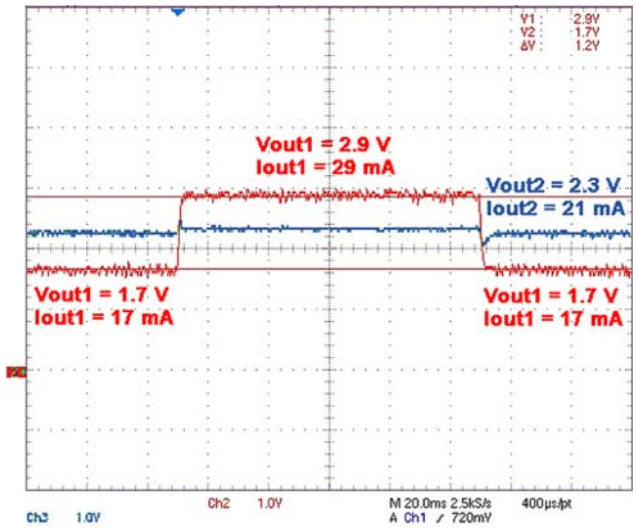

Fig. 12 Measured step response ($V_{OUT1} = 1.7$ V–2.9 V–1.7 V, $V_{OUT2} = 2.3$ V)

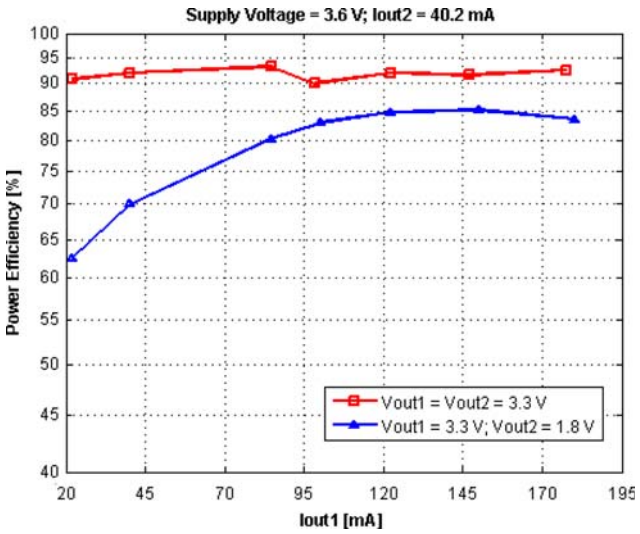

Fig. 13 Measured power efficiency ($V_{dd} = 3.6$ V, $I_{out2} = 40.2$ mA)

changing by 1.2 V (from 1.7 V up to 2.9 V and again down to 1.7 V). Also in this case, the power supply voltage value is equal to 3.6 V. The current on the first load increases and decreases by 12 mA (from 17 to 29 mA and from 29 to 17 mA). The variation of the first output in this case induces an increase of about 50 mV in the value of the second output. This behavior can be ascribed to the asymmetry of the control strategy. Indeed, the first output V_{OUT1} of the system is the favorite one, since the control of the inductor duty-cycle is based on its error.

Figure 13 shows the measured power efficiency of the system. By keeping the power supply set to 3.6 V and the output current on the second load equal to 40.2 mA, the power efficiency, measured as a function of the first output current, reaches 93.3% when both output voltages are set to 3.3 V and the overall output current is 124.8 mA. When the output voltages are set to 3.3 and 1.8 V, respectively, the power efficiency reaches 85.2% when the overall output current is 190 mA. The power efficiency is anyway always higher than 62.5%.

The system power efficiency as a function of both output currents is depicted in Fig. 14(a). The power supply voltage value and both output voltages are set to 3.6 and 3.3 V, respectively. It can be noted that for light loads the power efficiency is about 88%, while for medium-high loads it reaches values as high as 93%. When setting the second output voltage to 1.8 V, keeping constant all other voltage values, the measured system power efficiency is shown in Fig. 14(b). As in the case of Fig. 12, the asymmetry of the control strategy adopted is evident. In particular, when the current required from the first load is higher than the current on the second load, the system power efficiency reaches 88%, while this value decreases to 74% when

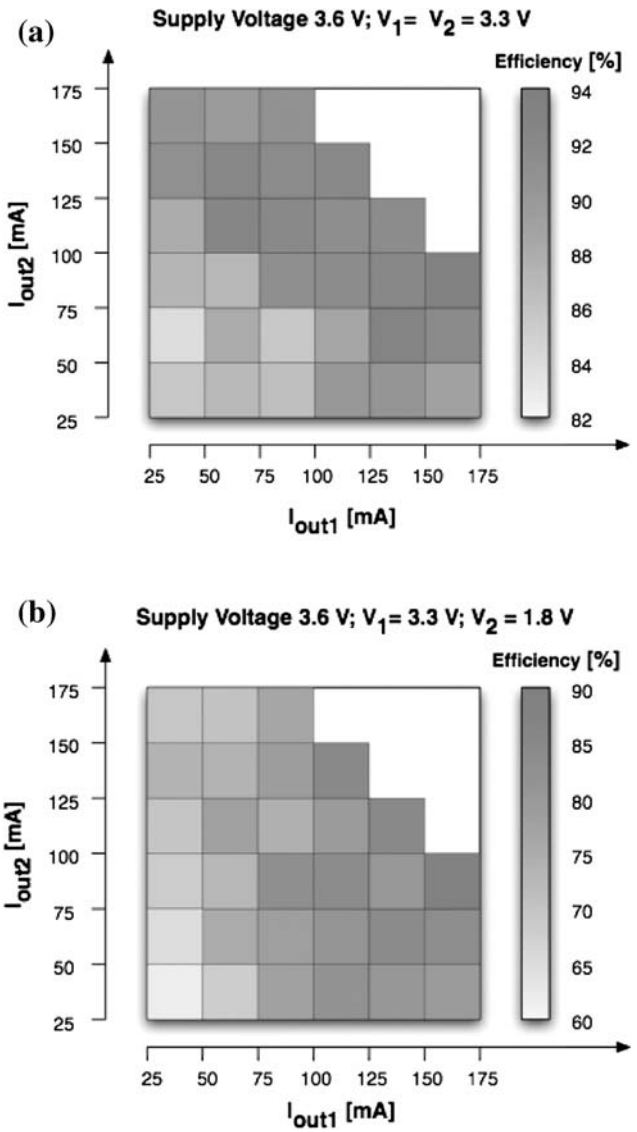

Fig. 14 Measured power efficiency. **a** $V_{dd} = 3.6$ V, $V_1 = V_2 = 3.3$ V; **b** $V_{dd} = 3.6$ V, $V_1 = 3.3$ V, $V_2 = 1.8$ V

the current delivered to the second load is higher than the one provided to the first load. The power efficiency measurements of Figs. 13 and 14 show that for low output currents, the converter efficiency drops. This is a typical limit of PWM-based DC–DC converters. However, Pulse Frequency Modulation (PFM) [12] can be used also in this two outputs buck converter to improve light loads efficiency.

Finally, in order to validate the simple behavioral model of the presented DC-DC buck converter discussed in the previous Section, several measurements have been performed. Indeed, circuits *BB1* and *BB2* in Fig. 3 can be disabled, thus connecting the wells of M_2 and M_3 to the supply line. In this way, it is possible to experimentally

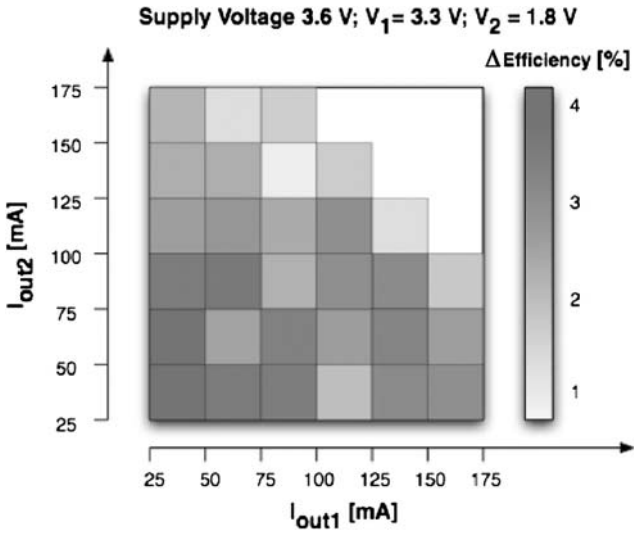

Fig. 15 Measured power efficiency with and without bulk biaser circuits

evaluate the effective improvement of the power efficiency performance that can be ascribed to bulk biaser circuits. Figure 15 shows the difference of the system power efficiency values obtained with bulk biaser circuits turned on and disabled. For light loads the improvement in power efficiency reaches 4.2%. This value decreases to 2% for high loads, in good agreement with the developed SIDO converter mathematical model (Fig. 7).

5 Conclusions

In this paper a novel single inductor dual output DC–DC buck converter has been presented. The proposed circuit, whose features are summarized in Table 1, by using only one (external) inductor, provides two independent output voltages ranging from 1.2 V to the power supply, which can vary from 2.6 to 5 V. The system overall current driving capability is 200 mA. An automatic substrate bias switch technique, that cancels the body bias effect of the p-channel output power transistors, improves the converter power efficiency performance. The proposed circuit has been fabricated in a 0.35-μm p-substrate CMOS technology. Measurement results demonstrate the effectiveness of the approach, showing that a power efficiency as high as 93% can be achieved.

Table 1 Performance summary

Supply voltage range (V_{in})	2.6–5 V
Regulated output voltages	1.2 V − V_{in}
	1.2 V − V_{in}
Switching frequency	1 MHz
Output capacitors (off-chip)	35 μF
Inductor (off-chip)	22 μH
Overall output current range	0–200 mA
Maximum power efficiency	93.3%
BB power efficiency improvement	2–4.2%
Technology	0.35-μm p-substrate (3-metal, 2-poly)
Chip area	1,350 μm × 1,800 μm (including pads)

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