Data Retention of Partial-SET States in Phase Change Memories

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Abstract—A key issue in non-volatile storage is long-term data retention. This aspect is even more important in innovative storage technologies, such as phase change memory (PCM), which promises better performance with respect to traditional Flash memory. In this work, we experimentally investigate the effects of the width and the amplitude of programming pulses on the degradation of intermediate programmed resistance levels over time in PCM cells, with the aim to contribute to the development of data retention-optimized algorithms for multilevel (ML) storage in PCM.

I. INTRODUCTION

Phase change memories are gaining increasing interest among innovative non-volatile memory technologies due to fast read access, short programming time, bit-level programming granularity, high endurance, good compatibility with standard CMOS fabrication processes, and potential of scalability beyond Flash technology [1].

The PCM working principle relies on the physical properties of chalcogenide alloys (typically Ge2Sb2Te5, GST) which can be reversibly switched between two structural phases having different electrical resistivity: the amorphous phase (highly resistive) and the (polycrystalline) phase (less resistive). The storage element of a typical PCM cell is composed of a thin GST film which is contacted by a resistive element (usually named heater). The phase transition takes place in a portion of GST referred to as the active volume, and is induced via proper thermal stimulation achieved thanks to Joule heating effect. Thus, the temperature inside the GST material can be indirectly controlled by means of electrical pulses applied to the cell. Typically, a PCM cell is programmed in single-bit per cell mode (bilevel storage): the active GST volume is either made completely amorphous (full-RESET state) or completely crystalline (full-SET state). The considerably large difference between the maximum ($R_{\text{RESET}}$) and the minimum ($R_{\text{SET}}$) cell resistance allows adequate margin for safe program and read operations in bilevel storage and opens the way to multilevel (ML) approach, where the cell is programmed to one of N>2 predetermined resistance levels in the range between $R_{\text{SET}}$ and $R_{\text{RESET}}$ (referred to as the read window). In the literature, two approaches have been proposed in order to program the cell resistance to an intermediate level: the SET-to-partial-RESET [2], [3] programming and the RESET-to-partial-SET programming [4]. In this paper, the second approach is considered: first, the cell is brought in the full-RESET state and, then, a partial-SET programming pulse is applied.

ML storage requires the cell resistance to be programmed and read with higher accuracy with respect to bilevel storage. In fact, the intermediate resistance values are closer than the two levels in bilevel storage, which are placed at upper and lower edge of the read window, respectively. In this respect, it should also be pointed out that each resistance level is affected by statistical spreads, due to fabrication process and programming variability. In addition, ML approach raises critical issues related to the retention of stored data, which is related to the shift of the programmed resistance levels over time.

Two phenomena affect the stability of the programmed resistance levels in PCM: the amorphous-GST drift [5] which leads to a resistance increase with time, and the crystallization process [6], which causes a resistance decrease. In this paper we focus our attention on the crystallization phenomenon which takes place in partially SET cells.

The crystallization process has been extensively investigated considering the bivolev case [7]-[8], where the crystallization process in the RESET state is the only responsible for data loss. The aim of this paper is to study data retention in the ML case and analyze the impact of the programming operation on the residual amorphous phase (i.e., on the phase which is still amorphous at the end of the partial-SET programming pulse), considering some parameters of the programming algorithm, such as the amplitude and the width of programming pulses. In order to separate the drift contribution from the crystallization one, we first characterized the drift dynamics in the considered partial-SET states and, then, corrected our data retention measurements.

The considered PCM chip is a 4-Mb array of µTrench cells with MOS selector [9], fabricated in 180 nm CMOS technology (see Fig.1a). The PCM cell is biased by applying adequate voltage levels to the selected bit-line (BL) through a high-voltage natural NMOS transistor, $V_{\text{DD}}$ which operates as a source follower. More specifically, voltage pulses having an amplitude $V_{\text{GST}}$ and $V_{\text{SET}}$ are applied to the gate terminal of $V_{\text{GST}}$ for RESET and SET operations, respectively. Reading is performed by sensing the current, $I_{\text{read}}$, flowing through the cell (hereinafter referred to as cell current) when a suitable read voltage $V_{\text{read}}$ (700 mV) is applied to the gate terminal of $V_{\text{GST}}$. Direct memory access (DMA) is allowed for characterization purposes.

II. EXPERIMENTAL RESULTS AND DISCUSSION

We first measured the drift coefficient $\alpha$ at room temperature (20 °C) considering different initial GST states. Since partial-SET programming gives rise essentially to a parallel phase distribution [10], we chose to analyze the drift and retention of the GST conductance ($G_{\text{GST}}$) rather than the GST resistance.

Our experimental procedure consists in the following sequential steps. We carried out a full-SET operation on an array of 2048 cells and, then, applied a full-RESET 100-ns voltage pulse (5.2 V) to all cells. We obtained the GST conductance by sensing the read cell current in DMA mode (heater contribution was removed after measurements). After the initial RESET operation, we programmed the considered cells by means of a single pulse having predetermined amplitude and time duration. Then, we measured the programmed cell conductance every 3 minutes over a time interval of about 30 minutes to characterize the drift dynamics. To this end, we assumed a power law dependence of the drift over time, as in the case of partial-RESET states [11], obtaining the following equation for the drift dynamics

$$G_{\text{GST}} = G_{\text{GST,0}} (t/t_0)^{-\alpha}$$

where $G_{\text{GST,0}}$ is the GST conductance value measured at time $t_0$. The calculated values of $\alpha$ are plotted in Fig. 1b.
After drift measurements, we baked the PCM device for 24 hours at 125 °C, and, finally, measured again the GST conductance, $G_{\text{GST}}$. On the basis of our drift measurements, we estimated the equivalent room temperature drift time of the bake operation, according to [12] and adequately corrected our retention measurements. Raw data is compared to corrected data in Fig.2. It can be noticed that the shape of the scattered data is not affected by the drift correction. The absolute variation of the GST conductance due to crystallization during bake is depicted in Fig. 3 for different values of partial-SET pulse duration. We experimentally observe a dependence of retention properties upon the achieved conductance when considering specific values of the amplitude and the width of the programming pulse. Moreover, our results suggest that programming thermal stress on the residual amorphous phase that surrounds the crystalline path affects the retention properties of partial-SET states. In particular, retention properties degrades as the programming thermal stress is increased. On the basis of our experimental analysis, similar conclusions can be drawn when comparing data obtained with partial-SET pulse having fixed time duration and different amplitude. In this case, data retention properties degrades as the amplitude of the programming pulses increase.

III. CONCLUSIONS

Our experimental analysis reveals a dependence of the retention properties on the programming operation, showing that retention degrades as programming thermal stress increases. This evidence suggests that data retention must be considered when developing multi-level programming algorithms.

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REFERENCES