Instrumentation for Gate Current Noise Measurements on sub-100 nm MOS Transistors

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Abstract

This work describes a measuring system that was developed to characterize the gate current noise performances of CMOS devices with minimum feature size in the 100 nm span. These devices play an essential role in the design of present day mixed-signal integrated circuits, because of the advantages associated with the scaling process. The reduction in the gate oxide thickness brought about by CMOS technology downscaling leads to a non-negligible gate current due to direct tunneling phenomena; this current represents a noise source which requires an accurate characterization for optimum analog design. In this paper, two instruments able to perform measurements in two different ranges of gate current values will be discussed. Some of the results of gate current noise characterization will also be presented.

I. INTRODUCTION

In the last decade, the requirements of high granularity in the design of the readout electronics for HEP experiments have led to an extensive use of deep-submicron CMOS processes. While approaching the 100 nm span, the CMOS technology has entered the sub-3 nm gate oxide thickness regime. In such a regime, MOSFET devices exhibit a non-negligible gate-leakage current, due to the finite probability of electrons directly tunneling through the insulating SiO\textsubscript{2} layer [1].

![Gate Current Density vs. Gate-to-Source Voltage](image)

Figure 1: gate current density of NMOS devices with various gate dimensions and belonging to two CMOS technology nodes, with different oxide thicknesses $t_{\text{OX}}$.

As an example, Fig. 1 shows the gate current density for NMOS devices belonging to two CMOS processes with 90 nm and 130 nm feature size; in the 90 nm process the leakage current is about 2-3 orders of magnitude higher than in the 130 nm process. This leakage current, which originates from discrete charges randomly crossing a potential barrier, is affected by noise fluctuations which may degrade circuit performance in analog applications.

In particular, in solid state detector readout circuits integrated in sub-100 nm CMOS technologies, the resolution, which is limited by the noise from the input transistor of the charge sensitive amplifier, may be degraded by the parallel noise source in the device gate current. In order to evaluate the effects of this noise contribution on the resolution of readout circuits, and to supply suitable design criteria for IC designers, accurate characterization and modeling of gate current noise are mandatory.

In this work, the noise characterization carried out by means of purposely developed instrumentation with the required accuracy in a frequency range large enough to include both white and 1/f or Lorentzian-like components, considering the dependence of the gate current from device geometry and bias conditions. This measuring instrument consists mainly of a transimpedance stage amplifying the noise in the DUT (device under test) gate-leakage current, which is converted into a voltage signal and than detected by a commercial spectrum analyzer. The constraint for the minimum detectable noise is chiefly dictated by the noise of the amplifier and its feedback resistor: the value of such a component has been chosen as a compromise between accuracy and bandwidth of the measuring system. As a result, the system allows for measurements from 0.1 Hz up to 100 kHz. Such a bandwidth allows us to fully characterize the gate current noise, which exhibits white, 1/f and Lorentzian-like behavior in this frequency range.

In order to measure the noise arising from an extended range of gate current values, two different interface circuits whose resolution has been optimized for two different intervals of these values have been developed.

After presenting the details of the interface circuit design and of the setup and procedures for gate noise measurements, results relevant to transistors belonging to a 90 nm and 130 nm CMOS technologies will be also presented and discussed.

II. GATE-LEAKAGE CURRENT NOISE

In MOS devices with ultrathin gate oxide thickness, direct tunneling appears to be the dominant mechanism of gate-leakage current. This current can be divided into three major contributions [2]: the gate-to-inverted channel current ($I_{gc}$), the
gate-to-source ($I_{gs}$) and the gate-to-drain ($I_{gd}$) components due to the path through the source and drain overlap regions. The gate-leakage current noise performances of a CMOS device can be characterized in terms of the gate noise current spectrum, which can be modeled by means of the equation [3]:

$$S_{2p}^2 = S_{W}^2 + \frac{A_{fg}}{\alpha_{fg}}$$  (1)

The first term in (1) describes the white noise component of the spectrum while the second one is given by flicker noise, where $A_{fg}$ is a power coefficient of the $1/f$ noise while $\alpha_{fg}$ determines the slope of this low frequency noise contribution. The term $S_{W}^2$ in (1) can be expressed by means of the well known shot noise law [4]:

$$S_{W}^2 = 2qI_G$$  (2)

where $I_G$ is the sum of the absolute values of each gate current contribution for a given bias condition.

### III. INSTRUMENTATION FOR NOISE MEASUREMENTS

In this section two interface circuits used to perform noise measurements will be presented. These circuits have been designed with different resolution on the basis of the expected noise level for a given gate current of the DUT.

![Figure 2: system for the noise measurements.](image)

The driving criterion in the design of the amplification systems was the minimization of their input-referred noise with respect to the current noise of the DUT, $S_{I,DUT}$. Noise experiments are performed by means of the system described in Fig. 2. The noise in the gate current of the DUT is converted into a voltage by means of a low noise transimpedance amplifier, and then detected by a commercial network/spectrum analyzer. The test signal source of the analyzer is applied, through the resistor $R_{GD}$ and the switch $S$, to the input of the interface circuit, in order to evaluate the transfer function of the measuring system. The transfer function is obtained by applying a voltage signal, converted into a current signal by means of the resistor $R_{FDT}$ shunted to the amplifier input virtual ground. The equivalent input noise current spectrum is calculated by dividing the output noise spectral density by the measured transfer function and taking into account the value of the resistor $R_{FDT}$. By means

$$G(j\omega) = \frac{R_F}{1 + j\omega R_F C_F},$$  (3)

The frequency response of the interface circuit is shown in Fig. 4, for a feedback resistor of $2 \, M\Omega$.
A noise analysis of the measuring system can be carried out considering the main noise sources, shown in Fig. 5, where $S_{I,RF}$ and $S_{I,RG}$ are current noise sources relevant to the thermal noise of the $R_F$ and $R_G$ resistors, while $S_{I,OP}$ and $S_{V,OP}$ are the equivalent input noise sources of the amplifier.

The noise of the measuring system can then be modeled by means of an equivalent input current noise source, whose power spectral density is given by the following equation:

$$S_{IYS}^2(\omega) = 4kT \left( \frac{1}{R_F//R_G} \right) + S_{I,OP}^2(\omega) + S_{V,OP}^2(\omega) \left( \frac{1}{R_F//R_G} \right)^2 \cdot \left[ 1 + \left( \frac{R_F R_G}{R_F + R_G} \right) \left( C_D + C_F \right) \right]^2,$$

(4)

where $k$ is the Boltzmann’s constant and $T$ the absolute temperature. Expression (4) can be minimized choosing high value resistors; the choice for the operational amplifier used in the transimpedance stage has been dictated by its performances in terms of parallel input-noise $S_{I,OP}$.

With the values used for $R_F$ and $R_G$, $I_{G,min} = 52 \text{ nA}$.

**B. Interface circuit for low DUT gate currents**

Measurements of noise spectral density arising from smaller currents, can be carried out by decreasing the noise contributions in the interface circuit. A solution which suitably improves the noise performance of the amplifying system is described in Fig. 7. The main difference with respect to the schematic of Fig. 3 lies in the absence of the gate-biasing resistor $R_G$, which leads to a significant noise reduction in the interface amplifier. In particular, the dominant noise source in this configuration is represented only by the feedback resistor $R_F$. Adopting a 100 $M\Omega$ resistor, it is possible to measure the noise arising from a minimum gate-leakage current in the order of few nanoamps, as highlighted in Fig. 8, where the signal-to-noise ratio ($S_{I,DUT}^2/S_{IYS}^2$) equal to unity:

$$I_{G,min} \approx \frac{4kT \left( \frac{1}{R_F} + \frac{1}{R_G} \right)}{2q}.$$

(5)

With the values used for $R_F$ and $R_G$, $I_{G,min} = 52 \text{ nA}$.
At low gate current, the noise at the output of the transimpedance amplifier requires an additional gain stage in order to overcome the noise of the spectrum analyzer; in particular, a 40 dB gain stage has been included in the circuit. Resistor \( R_0 \) and capacitor \( C_0 \) perform the high-pass filtering action needed to decouple the two stages of the circuit. Adequate values for these components were chosen in order to obtain an extremely low cut-off frequency. Stray capacitor \( C_A \) in parallel with resistor \( R_A \) introduces an high-frequency pole in the frequency response of the system. The value of the feedback resistor \( R_F \) of the transimpedance amplifier has to be chosen as a compromise between the noise performance of the measuring system and the range of the gate current values in the DUT, which is limited by the output dynamic range of the amplifier. Fig. 9 shows the good agreement between measured and theoretical frequency response, which can be calculated as follows:

\[
G(j\omega) = \frac{R_F}{1 + j\omega R_F C_F} \left( 1 + \frac{R_A}{R_B} \right) \frac{1 + j\omega \left( \frac{R_A R_B}{R_A + R_B} \right) C_A}{1 + j\omega R_A C_A}. \tag{6}
\]

IV. NOISE MEASUREMENTS

The instruments described in Section II were used to measure gate-leakage current noise of devices belonging to a 130 nm and a 90 nm CMOS process by STMicroelectronics. Noise was measured by means of a HP3562A Dynamic Signal Analyzer, also performing network transfer function characterization.

Fig. 10 and Fig. 11 show noise current spectra of NMOS with different dimensions biased in different conditions in terms of gate-to-source and drain-to-source voltages, for gate current values ranging from 0.8 nA to 4.9 µA. Source and bulk of the DUTs was always connected to ground.

Noise measurement results have shown that the gate current noise spectrum exhibit both white and \( 1/f \) behavior, therefore they can be modeled by means of equation (1). The results show a dependence of the \( 1/f \) term on the gate current: decreasing the gate-leakage current of the DUT results in a lower \( 1/f \) noise contribution.
This low-frequency noise exhibits a quadratic dependence on the gate current [5]. For devices belonging to the 130 nm process the $1/f$ noise component of the spectrum is not clearly visible at 1 Hz as shown in Fig. 11 b), while the white noise contribution confirm the good accuracy of the model for the theoretical behavior expressed by (2). In order to detect $1/f$ contribution it has been necessary to perform measurements from lower frequencies, as shown in Fig. 11 c), relevant to a gate current smaller than 1 nA. As it can be seen in the presented spectra, white and $1/f$ noise increase by increasing the gate current; moreover, at a fixed current, white noise seems to be almost independent of the gate geometry. Some devices exhibited Lorentzian-like noise behavior, as shown in Fig. 11 d).

V. CONCLUSION

This paper described a laboratory instrument for gate-leakage current noise measurements that is an effective tool for the characterization of CMOS devices with oxide thickness in the 2-nm span. In the frequency range used for the presented results, it was possible to fully characterize the noise behavior of the DUTs. Measuring the $1/f$ noise component in extremely low gate currents (a few nanoamps or less) requires measuring the DUT noise spectrum from very low frequencies as the flicker term rapidly decreases with the gate-leakage current. With this instrumentation it is possible to carry out a complete characterization of the technologies used in the design of low-noise charge sensitive amplifiers, where the gate-leakage current can represent a limit in the achievable resolution.

REFERENCES


