24.3 A Reconfigurable Demodulator with 3-to-5GHz Agile Synthesizer for 9-Band WiMedia UWB in 65nm CMOS

Andrea Mazzanti¹, Mohammad B. Vahidfar², Marco Sosio³,
Francesco Svelto³

¹University of Modena and Reggio Emilia, Modena, Italy

²Istituto Universitario Studi Superiori di Pavia, Pavia, Italy

³University of Pavia, Pavia, Italy

Receiver ICs realized in CMOS technology leverage the narrowband nature of wireless standards to meet specifications at low power levels. The advent of wideband systems, e.g. software-defined radios and UWB technology, is determining new emphasis on innovative techniques for key RF circuit blocks, and on synthesizers in particular [1-4]. Ring-oscillator-based solutions lend themselves to wideband operation but the signal quality at moderate power consumption is usually inadequate, while LC-tank-based oscillators do not cover the range requiring multiple VCOs. Sum and difference frequencies can be generated from a single VCO and its divided replica by means of SSB mixers. Unfortunately, significant spurious tones are created due to non-idealities in the mixers. As an alternative, RF signals belonging to a wide frequency range can be demodulated in a single receiver chain by means of a downconverter, reconfigured between conventional and subharmonic operation modes. In this way, the local oscillator is required to cover only a fraction of the frequency range, demodulating the lower portion in conventional mode and the upper in subharmonic mode. For subharmonic downconversion, 4 differential phases of the same reference are needed but the advantage of the lower frequency range of operation outweighs the added complexity.

In this paper, a 65nm CMOS reconfigurable direct-conversion receiver, tailored to WiMedia UWB (band groups 1,3 and 4) including frequency synthesizer, mixer and baseband first stage is described. Experiments show a robust operation while the synthesizer requires a record low 43mW dc power.

Figure 24.3.1 shows the diagram of the quadrature passive mixer, which is the core of the proposed demodulator. The input RF current is downconverted to DC by means of two stacked double-balanced switching stages. Differential reference signals driving each stage are provided according to the phase sequence reported in the figure. When either of the two stages is set to a constant biasing while the other switches at the LO frequency, the downconverter operates in conventional mode, and the output frequency equals $\omega_{RF}-\omega_{LO}$. When the two stages are switched at the same LO frequency by reference signals phase shifted by 90°, the output frequency equals $\omega_{RF}-2\omega_{LO}$. The multiple-phase reference is generated by a ring oscillator and a phase selector reconfigures the mixer for either operation mode. Figure 24.3.2 shows the block diagram of the proposed solution. In order to demodulate UWB band groups 1,3 and 4 the required frequency ranges for the demodulator and the LO generator are 3.1 to 9.5GHz and 3.3 to 4.62 GHz, respectively. To provide a spectrally pure, low-phase-noise reference, the ring oscillator is injection locked by an LC-VCO-based PLL. Due to the specified fast frequency hopping within a 3-band group, the system is intended to operate with 3 separate PLLs each dedicated to a single band. In the present implementation, only two have been integrated while the third input provides a reference generated off-chip for testing purposes. When locked, the output signals of the ring oscillators maintain the desired relative phase difference of exactly 45° only if the free-run frequency is the same as the locking frequency. Digital calibration of the oscillation frequency is therefore included, together with a set of registers to store the calibration words for each channel frequency. The signal determining which of the three PLLs locks the ring also selects the corresponding calibration word.

The detailed schematic of the ring oscillator is shown in Fig. 24.3.3. Each delay cell is made of a differential pair and binary-weighted switched-pMOS loads, working in the linear region. Eight control bits are used to achieve a frequency resolution of less than 20MHz, fine enough to keep the deviation from nominal phase difference to less than 0.5° in the locked condition. To maintain a constant output swing at different frequencies, current consumption is

automatically regulated by a replica biasing circuit. The locking signal is provided to the ring by means of an additional differential pair shunting a delay cell. Locking bandwidth is set by its tail current (I_{inj}). The larger I_{inj} , the larger the locking bandwidth, i.e. the better the ring phase noise suppression, but the less the phase accuracy due to the asymmetries introduced in the loop. I_{inj} is set for a locking bandwidth of 1.5GHz as the best compromise. The on-chip PLLs use an integer-N architecture employing a reference frequency of 66MHz. LC-VCOs cover the required frequency range in 8 overlapping bands. Frequency dividers are implemented with a divide-by-two CML stage followed by a pulse-swallow counter. Maximum current consumption is 5mA for each PLL. The front-end RF transconductor is implemented by means of a differential pair biased with a center-tapped choke inductor. The baseband transimpedance amplifier shown in Fig. 24.3.3 is realized using a unity current gain common-gate stage with a differential output load, resulting in a first order filter.

The die micrograph of the circuit, fabricated in the STMicroelectronics 65nm CMOS process, is shown in figure 24.3.7. The chip draws 66mA from a 1.2V supply. The ring oscillator free-run frequency is digitally programmable between 3 and 5.6GHz. During characterization the ring is locked by the PLLs. Frequency hopping within the same group sets 9.5ns as maximum allowed band-switching time, determined by multiplexer delay plus ring locking transient in our solution. A settling time of less than 6ns has been measured when switching the LO frequency between 3.432 and 3.960GHz and down-converting a 3.372GHz RF signal to base-band, as shown in Figure 24.3.4. The phase noise at 10MHz offset from 3.96GHz is -128 dBc/Hz, determined by the injecting LC PLL. Integrated phase noise is less than 1.7°. Keeping low spur levels to avoid downconversion of undesired interferers is key. Figure 24.3.5 shows the spectrum at synthesizer output when the ring is locked to 3.960GHz by PLL2 while PLL1 and the external PLL are 528MHz apart on the two frequency sides. The largest spurs, due to the two side PLLs, are -43dBc. Spurs around the synthesized frequency are due to the reference and its harmonics, while no spurs are present in the 5-to-6GHz WLAN range.

The demodulator gain is 10dB both in fundamental and subharmonic operation modes, and the output frequency pole is at 300 MHz. A rapid 4dB gain decrease is observed in the last bands (8.7 to 9.5GHz), attributed to the PCB frequency response. The deviation from quadrature of I and Q downconverted signals is less than 2°. Input-referred noise-voltage spectral density is 2.3 nV/√Hz. Out-of-band linearity tests have been performed: 1dBV IIV3 (11dBm IIP3 on 50Ω), with tones at 5.2 and 5.8GHz, and 30dBV IIV2 (40dBm IIP2 on 50Ω), with tones at 1.9 and 5.2GHz, have been derived. Figure 24.3.6 summarizes measured results.

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Figure 24.3.1: Reconfigurable quadrature passive mixer.

Figure 24.3.2: Block diagram of the I & Q demodulator and frequency synthesizer.

Figure 24.3.3: Ring oscillator and baseband transimpedance amplifier.

Figure 24.3.4: Demodulator settling time. The LO frequency is switched between 3.432 and 3.960GHz while a 3.372GHz RF signal is downconverted to baseband.

Figure 24.3.5: Local Oscillator output spectrum when PLL2 locks the ring at 3.96GHz while PLL1 and the external PLL are 528MHz apart. Spurs around 8GHz are 2nd harmonics generated by the single-ended measurement buffers.

Performance Summary

Gain [dB]	10
Input Referred Noise [nV/√Hz]	2.3
IIP3 [dBm]	11
IIP2 [dBm]	40
I & Q phase error [deg]	< 2
Phase Noise @ 10 MHz [dBc/Hz]	-128
Integrated Phase Noise [deg]	< 1.7
Spurs Level [dB]	-43
Frequency Hopping time [ns]	< 6ns
Power Consumption [mW]	79
Silicon Area [mm ²]	3.7 (1.5 Active)
Technology	CMOS065

Figure 24.3.6: Performance summary.

Figure 24.3.7: Chip micrograph.