A 13.1% Tuning Range 115GHz Frequency Generator Based on an Injection-Locked Frequency Doubler in 65nm CMOS

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Ultra-scaled CMOS devices offer the possibility of operation beyond 100GHz where new applications are envisioned in the near future, including imaging and spectroscopy systems for scientific, medical, space, and industrial applications at low cost, light weight and easy assembly [1]. However, a long path toward complete systems of any commercial interest is required, even though simple building blocks have already been presented [2-6]. One of the challenges of such high-frequency transceivers is the on-chip reference generation. Adoption of a voltage-controlled oscillator (VCO) at fundamental frequency sets an increasingly severe trade-off between high spectral purity and frequency tuning due to a dramatic reduction of resonator quality factor and large parasitics introduced by active devices and buffers, operating close to the transition frequency. As an example, state-of-the-art varactor-tuned VCOs beyond 100GHz in standard CMOS technology display a tuning range of less than 3%, not enough to cover process spreads [3-5]. An alternative solution relies on frequency multiplication of a lower frequency reference, with the potential advantage of a higher tuning range and lower phase noise set by the lower frequency VCO enslaving the multiplier.

In this paper a low power 115GHz CMOS injection-locked frequency multiplier-by-two with a differential output is presented. Prototypes, realized in a standard 65nm CMOS technology, provide 300mV single-ended peak voltage swing, while drawing 6mA from a 1V supply. When combined with an integrated half-frequency VCO, the on-chip reference demonstrates a phase noise of -107dBc/Hz@10MHz offset with a 13.1% tuning range.

The schematic of the injection-locked frequency multiplier is shown in Fig. 23.5.1. The C-L-C network and transistor Mₙ form a standard Pierce oscillator. Transistors M₁-M₂, connected in push-push configuration, i.e. with the drains and sources connected in parallel and the gates driven by signals in opposite phase, inject a current in the resonator node 1 at twice the input signal frequency to lock the oscillator. Compared to a stand alone push-push pair driving a tuned load, compared to a stand alone push-push pair driving a tuned load, the proposed solution provides a differential output and, due to the positive feedback in the oscillator, injection locking leads to higher output swing. The frequency locking range is primarily set by the ratio between the two biasing currents, I₂ and I₁. Assuming 300mV input swing, and the two currents set to 3mA, the oscillator is locked over a bandwidth of 19% around 115GHz center frequency.

Capacitor C_CM is introduced to balance the two output voltages, V₁ and V₂. In fact, even if transistor Mₙ sets 180° between V₁ and the current I₁ injected in the resonator node 2, the two ports of the C network are not driven symmetrically and the outputs are not balanced. Capacitor C_CM suppresses the output common-mode voltage V_CM. As an intuitive view, V_CM is shorted to ground by the low impedance provided by the series resonator formed by C_CM and the L/2 branch. To gain insight, the outputs of the free-running oscillator without C_CM display a phase deviation from 180° larger than 15° which reduces to less than 1° when C_CM is introduced. Good output balancing is maintained also when the circuit is locked with an offset from the free-run frequency. From post-layout simulations, phase error between the two output voltages of the locked multiplier is less than 5° over the band of ±10% from the free-run frequency.

The multiplier core transistors, M₁ and M₂, are biased at a constant DC current, set by the two current mirrors M₃, which capacitors C₃ are large enough to behave as AC shunts. The supply to the circuit is provided through a choke inductor (Lₜ) to the center tap of the resonator. To maximize the series impedance and the self-resonant frequency, it is realized as a 3.5 turns spiral of a thin 0.4µm width trace in the topmost metal only. Grounded capacitors, in Fig. 23.5.1, are explicitly required in each node for proper operation and absorb all device parasitics, making the circuit particularly suited for very high operation frequency.

For measurement purposes, the multiplier drives a two-stage buffer, shown in Fig. 23.5.2. The first stage is a differential common-source pair (M₁₂) with inductive loads while the second is a differential pair (M₄₅), supplied off chip with bias tees, driving the 50Ω load of the measurement setup. If an off-chip local oscillator (LO) signal is superimposed to the bias voltage of the tail transistor (M₅), the latter works as a downconversion mixer translating the multiplier output signals at a lower frequency.

Two different chip versions have been realized. In the first, the multiplier is locked by an off-chip half-frequency reference. A lumped balun has been integrated to make the input signal differential. In the second version, the multiplier is locked by an on-chip half-frequency VCO. The latter is a standard nMOS differential pair LC-tank oscillator tuned with accumulation-mode MOS varactors and dissipates 6mW.

All measurements presented here have been performed by downconverting the signal to V-band (50 to 75GHz) on chip, where instrumentation is presently available. The setup for characterization of the first chip is shown in Fig. 23.5.3 (top). Agilent signal sources provide the input signal and the LO for the secondbuffer stage. The output is measured with a Spectrum Analyzer, extended to V-band through a compatible external harmonic mixer. The bottom plot shows the measured output spectrum, when the multiplier is locked to a 60GHz input signal of 0dBm and the 120GHz output is translated down to 70GHz with the external LO set to 50GHz. Figure 23.5.4 shows the measured single-ended power vs. the multiplier output frequency when the latter is driven by the external source and the on-chip VCO. Taking into account the estimated 16dB conversion loss of the on-chip mixer, the peak voltage swing at the multiplier output is -300mV. The fully integrated solution covers the band from 107 to 122GHz corresponding to a 13.1% tuning range. The single-ended voltage swing is always larger than 100mV. The two circuits consume a total power of 12mW. The free-running multiplier has a phase noise of -100 dBc/Hz@10MHz offset. When locked by the VCO, the measured phase noise profile is shown in Fig. 23.5.5 and, at 10MHz offset, it is reduced to -107dBc/Hz. Finally, the performances of the VCO and multiplier combination, proposed in this work, are summarized and compared against stand-alone fundamental frequency VCOs in the Table in Fig. 23.5.6. In the last column, the FOMₙ normalizes frequency, power dissipation, phase noise and tuning range [6]. The proposed solution shows more than 10dB improvement against state of the art.

Micrographs of the realized test chips are shown in Fig. 23.5.7.

Acknowledgments:

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References:

Figure 23.5.1: Schematic of the injection-locked frequency multiplier-by-two.

Figure 23.5.2: Schematic of the buffer/mixer cascading the multiplier.

Figure 23.5.3: Experimental setup (top) and typical output spectrum (bottom).

Figure 23.5.4: Measured power after on-chip downconversion to V-band versus multiplier output frequency. Amplitude at multiplier output estimates 16 dB higher.

Figure 23.5.5: Phase noise at the multiplier output when driven by the on-chip half-frequency VCO.

Figure 23.5.6: Performance summary and comparison of the VCO and multiplier against fundamental frequency VCOs.

<table>
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<th>Ref.</th>
<th>$f_0$ [GHz]</th>
<th>Phase Noise [dBc/Hz @ 1MHz]</th>
<th>Tuning Range [%]</th>
<th>Power [mW]</th>
<th>FOM$_f$ [dB]</th>
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<td>7</td>
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<td>7.6</td>
<td>-164.6</td>
</tr>
</tbody>
</table>

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$^*$32nm SOI-CMOS
Figure 23.5.7: Micrograph of the test chips.