Design of time invariant analog front-end circuits for deep n-well CMOS MAPS

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Abstract—This work is concerned with the design of time invariant analog circuits for processing the signals from deep N-well monolithic CMOS sensors. As compared to the three-transistor front-end typically used in imaging applications, the schemes proposed here, which were conceived to be included in a binary readout channel, lend themselves to pixel-level sparsified readout and are expected to be capable of managing the large flow of data anticipated for the future high luminosity colliding machines while obeying quite severe material budget requirements. Various solutions complying with different power dissipation and point point constraints have been implemented in a 130 nm CMOS technology, paying particular attention to equivalent noise charge and threshold dispersion performance. This paper intends to describe and compare the features of the different approaches by means of simulations, experimental results and theoretical analysis.

Index Terms—Charge preamplifier, thermal noise, flicker noise, threshold dispersion, MAPS sensors, CMOS processes.

I. INTRODUCTION

PHYSICS processes taking place at the future high luminosity colliding machines, like the International Linear Collider (ILC) and the Super B-Factory, will feature very high track densities and call for highly granular, multi-layered, light detectors to be placed very close to the beam interaction regions. As a response to these requirements, several research groups have been working in the past few years on adapting CMOS monolithic active pixel sensors (MAPS), mainly developed for imaging applications, to charged particle tracking [1], [2], [3]. The idea of using such devices for vertex detection purposes is mainly based on the following characteristics:

- the readout electronics (front-end and back-end) is fabricated in the same substrate as the detector;
- CMOS MAPS can be ground down to a few tens of microns with no significant signal loss, since their operating principle is based on the collection of charge diffusing in an undepleted substrate.

Both of the above features make CMOS MAPS potentially compliant with the stringent material budget requirements set by the next generation experiments to minimize multiple scattering across the detector layers and significantly improve momentum measurement accuracy. On the other hand, the very high degree of pixellation which will be featured by future vertex detectors also requires extremely large bandwidths. This is needed to manage the large data stream from the sensor matrix while maintaining detection efficiency at an adequate level. Therefore, data selection in some processing phase is considered mandatory to minimize the burden on the data acquisition system. In most of the proposed readout architectures for MAPS, the entire data content of the sensor matrix is read out sequentially or with a column parallel technique by means of a periodically reset source follower amplifier. ADCs and sparsification logic are generally placed in the chip periphery.

A different approach, which relies upon the properties of the triple well structures included in modern CMOS processes for NMOS transistor isolation, has been recently proposed. This led to the design and fabrication of the so called deep N-well (DNW) MAPS [4]. In these devices, a relatively (as compared to standard three transistor MAPS) large collecting electrode featuring a buried N-type layer is integrated with a classical, fully CMOS readout chain for time invariant charge amplification and shaping. This has to be compared with the typical, imaging-like approach, where correlated double sampling (CDS) techniques are used to perform time variant filtering. The DNW MAPS solution was intended to enable data driven readout, or at least zero suppression, directly at the elementary cell level. Actually, based on the proposed device, the first ever MAPS detectors with pixel-level sparsification have been designed and produced [5], [6]. The MAPS devices discussed in this work were fabricated in a 130 nm commercial process by STMicroelectronics. At the moment, this technology seems to offer the best compromise between achievable functional density and costs in view of the final production of a full scale monolithic detector. However, also more scaled technologies (90 nm and 65 nm minimum channel length) are being characterized and taken into consideration for CMOS MAPS design [7], [8]. At least in principle they may provide increased functionality, higher degree of radiation hardness and better noise/power trade-off.

This work aims at discussing the design features and performances of time invariant analog channels for signal processing in CMOS DNW MAPS and extends and completes the conference paper presented at the 2008 IEEE Nuclear Science Symposium [9]. With respect to previously published material...
on DNW MAPS, this paper is meant to present more recent results from the characterization of new versions of the device. Moreover, and most of all, it provides a theoretical comparison between the adopted analog front-end solutions and discusses some general criteria for optimum analog processor design. The paper is structured as follows. After this introduction, the second section of the work will be concerned with the analysis of the available technologies, including the DNW MAPS approach, enabling fully CMOS design of monolithic sensors. The third section will be devoted to studying the characteristics of a couple of solutions, both including a charge preamplifier and a shaping stage, which were proposed for applications to the vertex detector of the SuperB Factory and were integrated in the chips of the so called Apsel (active pixel sensor electronics) series. Particular care will be taken in discussing and comparing the threshold dispersion properties of the two proposed solutions. The fourth section will describe the features of a shaperless readout channel, integrated in a prototype chip (SDR0, sparsified digital readout) for vertexing applications at the ILC experiments. In the fifth section, optimum design criteria for shaperless analog processors in multichannel systems will be defined and discussed. The sixth and final section will be concerned with a comparison between the theoretical equivalent noise charge (ENC) and threshold dispersion performances of the shaperless solution and those of the analog channel with RC-CR shaper.

II. FULLY CMOS DESIGN OF MONOLITHIC SENSORS

Conventional MAPS in CMOS technology are based on a small-area, charge-collecting N-type diffusion on P-type substrate read out by simple front-end electronics including only NMOSFETs. Charge sensitivity is inversely proportional to the parasitic capacitance of the detector. Choice of a minimum area collecting diode serves the purpose of minimizing switching noise effects. However, due to the small dimensions of the sensing electrode, any PMOS device in the surroundings of the diode would dramatically reduce the charge collection efficiency of the pixel by stealing a significant part of the charge released in the substrate by the impinging particle. The DNW MAPS approach, still based on a standard CMOS technology, relies upon a relatively large area collecting electrode read out by a classical optimum chain for capacitive detectors. This includes a charge preamplifier, whose closed loop gain is independent of the detector parasitic capacitance. Use of a large area sensing diode makes it possible to integrate PMOS devices in the elementary cell, as long as the area covered by the PMOS N-wells is a small fraction of the sensing diode area. This paves the way for the design of fully CMOS analog and digital blocks, with significant advantages in terms of performance and power dissipation. However, in the design of DNW MAPS, care has to be taken that the area covered by PMOS devices is kept as small as possible and that the sensor is suitably laid out to enclose the charge-stealing N-wells. Complete freedom to use PMOS devices in the design of monolithic sensors is instead guaranteed by silicon on insulator (SOI) and, more recently, by quadruple well CMOS technologies. In SOI processes the device layer is electrically separated from the sensing volume by means of a buried oxide (BOX) layer, therefore radically eliminating the issue of charge sharing between the sensing diode and the parasitic N-well collecting electrodes. Generally, in the fabrication of SOI wafers for CMOS MAPS, a low resistivity device layer is bonded to a high resistivity (supporting) detector layer [10]. This makes SOI CMOS MAPS conceptually very similar to hybrid pixels, where a readout electronics chip is bump bonded to a fully depleted detector, with considerable benefits in terms of charge collection speed and efficiency. Several CMOS SOI MAPS prototypes have been fabricated, either based on specifically conceived, non standard processes [11] or on well established fully-depleted (FD) SOI technologies [10],[12], which anyway need additional steps for substrate implants and contact formation. A couple of issues in SOI MAPS design has still to find a final and satisfying solution. First, full depletion of the detector layer in an SOI MAPS involves applying a relatively high (several tens of Volts) back-gate voltage, which may strongly affect transistor threshold and impair its operation (back-gate effect). Further processing steps may limit threshold shift and keep devices working in high back-gate voltage conditions. Crosstalk between front-end circuits, especially digital blocks, and the sensor through the BOX layer, is the second pending issue in SOI MAPS. Crosstalk suppression may require adopting particular architectural (use of differential stages) and/or technological (sensor guard rings, use of double gate or Fin transistors) [10]. On the other hand, quadruple well technologies appear to be the most straightforward answer to the issue of parasitic N-well collection. They feature an additional deep P-well implant used to shield the N-well forming the substrate of PMOS devices. This option is presently available in a purposely developed 0.18 µm CMOS process [13]. However, at the moment, limited accessibility seems to be the main issue with quadruple well processes.

III. DNW MAPS WITH INTEGRATED CHARGE PREAMPLIFIER AND SHAPER

The Apsel series chips were designed and fabricated in the framework of the Italian SLIM5 collaboration, aiming at
the development of thin, high momentum resolution tracking systems for high energy physics (HEP) experiments. This R&D activity is in particular being carried out in view of vertexing applications at the Super-B Factory. In the Apsel chips, the elementary MAPS cells feature a 50 \( \mu \)m pitch and a power dissipation of about 30 \( \mu \)W/channel. Fig. 1 shows the layout of the Apsel3T1 chip (left) and of the Apsel3T2 chip (right), both including two 3 \( \times \)3 and one 8 \( \times \)8 matrices. With respect to the first Apsel prototypes, some substantial modifications have been made to the sensor and the front-end electronics. In both chips, the DNW sensor was laid out in such a way to reduce the parasitic capacitance \( C_D \) to about 300 fF (from more than 450 fF in the previous versions). Furthermore, the analog section and the substrate are shielded from the digital signals, routed through metal 5 and metal 6, by means of large metal 4 strips, also used for power distribution. The block diagram of the front-end electronics integrated in the elementary cell is shown in Fig. 2 together with some transistor-level details. The first stage of the processing chain is a charge preamplifier using a complementary cascode scheme as its forward gain stage, which is responsible for most of the power consumption in the analog section. The feedback capacitor \( C_F_1 \) is continuously reset by an NMOS transistor biased in the deep subthreshold region. The preamplifier input device, featuring an aspect ratio \( W/L=14/0.25 \) and a drain current of 20 \( \mu \)A, was optimized for the DNW detector capacitance. The charge preamplifier is followed by a bandpass filtering stage. A discriminator is used to compare the processed signal to a chip-wide preset threshold \( V_{t_0} \), therefore providing hit/no-hit information to the cell digital section. The pixel logic includes blocks for hit event storage and pixel-to-periphery communication enabling data driven readout and time stamping [6].

A. Shaping stage solutions

In the case of the filtering block, a couple of different solutions have been implemented and tested. The first one, an RC-CR (i.e. a first order semigaussian unipolar) shaper, was integrated in the Apsel3T1 test structures. It includes a transconductor stage in the feedback network (see Fig. 2 a)) and features a programmable peaking time, which can be set to 200 ns or 400 ns. The design of an RC-CR shaper for the readout channel of the Apsel deep N-well MAPS has been already fully covered in a previous work [14]. It is nevertheless worth recalling here that, if the shaper gain stage features a single pole transfer function \( T(s) \), with cutoff frequency \( f_0,s \) and DC gain \( T_0 \), and the condition

\[
\frac{GBP_s}{G_m} = \frac{4}{\pi} \frac{C_1 + C_2}{C_2^2}, \quad GBP_s = 2\pi T_0 f_0, \tag{1}
\]

is satisfied, then the closed loop shaper transfer function \( T_{cl}(s) \) becomes

\[
T_{cl}(s) = -\frac{2}{GBP_s} \frac{s t_p}{(1 + s t_p)^2}, \tag{2}
\]

where the peaking time \( t_p \) is given by

\[
t_p = \frac{2}{GBP_s} \left( 1 + \frac{C_1}{C_2} \right). \tag{3}
\]

In the previous equations, \( GBP_s \) is the shaper open loop gain-bandwidth product, \( G_m \) is the feedback transconductance, \( C_1 \) is the differentiating capacitance at the shaper input, \( C_2 \) is the capacitance in the shaper feedback network. Fig 3 shows the signal at the shaper output, acquired by means of a digital scope. This is the response to a 750 electron charge pulse injected by an Agilent 33250A Function / Arbitrary Waveform Generator through an integrated 60 fF MIM (metal-insulator-metal) capacitor. The response was measured for both
Fig. 3. Signal at the output of the Apsel analog readout channel when an RC-CR shaper is used as the bandpass filtering stage. The response was measured for the two available peaking times, nominally 200 ns and 400 ns.

Fig. 4. Signal at the output of the Apsel analog readout channel when a current mirror is used in the feedback network of the bandpass filtering stage. The response was measured for different values of the injected charge. The slight undershoot results from the differentiation of the non ideal response of the charge preamplifier, which is a slowly decaying exponential signal and not a step function.

As an alternative to the feedback network used in the classical semigaussian filter, a different one, shown in Fig. 2 b), was implemented in a second version of the shaping stage, which was integrated in the Apsel3T2 chip. It consists of an NMOS current mirror structure continuously resetting the shaper feedback capacitor $C_2$. Since $C_2$ is discharged by a constant current, proportional to the mirror reference current $I_{cm}$, the recovery time increases linearly with the signal amplitude. This filtering technique actually lends itself well to amplitude-to-time conversion, such as in time-over-threshold systems [15]. Fig. 4 shows the signal at the shaper output when a current mirror is used in the feedback network. The waveform was measured as a response to different values of the charge $Q_{inj}$ injected at the preamplifier input, for $I_{cm}=12$ nA. The peaking time, about 500 ns for $Q_{inj} < 500$ electrons, increases to about 800 ns for larger amounts of injected charge, pointing to a non linear behavior of the shaping stage. As in Fig. 3, the undershoot results from the differentiation of the preamplifier signal.

Full characterization of the two proposed solutions have been carried out, yielding the results shown in Table I. Charge sensitivity was evaluated by measuring the spectral response of single pixels to soft X-rays from an $^{55}$Fe radioactive source. A very simple setup was used for these measurements, including a digital scope, which is triggered by the signal exceeding a preset threshold and stores the relevant peak amplitude. The fairly high values shown in the table, quite in agreement with post layout simulations and of the order of 900 mV/fC, are instrumental in minimizing threshold dispersion effects. Equivalent noise charge was measured by evaluating (again by means of a digital scope) the noise root mean square at the shaper output, divided by the charge sensitivity, in a statistically significant number of single cells belonging to $3 \times 3$ matrices. ENC can be observed to decrease with increasing peaking time in the case of the analog channel with RC-CR shaper. This trend is confirmed by the current mirror solution, which features, as mentioned above, a peaking time of 500 ns or larger. Threshold dispersion was evaluated through threshold scan techniques in $8 \times 8$ MAPS matrices and was referred to the preamplifier input by taking into account the charge sensitivity. Firing efficiency curves at each of the 64 pixel digital outputs were measured by means of a Tektronix TLA 7PG2 Pattern Generator module, which was used to program an on-board 12 bit DAC setting the discriminator threshold and to enable the matrix parallel output one raw at a time. A 7AA1 34 Logic Analyzer module was used to acquire the data at the matrix output. The modules were integrated into a Tektronix TLA 700 Series mainframe. In order to accumulate a statistically significant amount of information for each point of the firing efficiency curves, the digital content of the 64 pixels was acquired 1000 times for each considered threshold value. Offline data analysis was used to extract the threshold dispersion figures. The obtained results, for both the RC-CR and current mirror solutions, also include contributions from the threshold discriminator, a differential NMOS pair with PMOS mirrored load [14]. The current mirror shaper was found to provide significantly better threshold dispersion performances than in the case of the RC-CR filter. Since this is one of the main reasons to prefer the current mirror to the

| TABLE I | CHARGE SENSITIVITY, ENC AND THRESHOLD DISPERSION FOR THE APSEL MAPS PROTOTYPES |
|---------|-------------------------------|-------------------------------|
|         | RC-CR shaper | Current mirror shaper |
| Charge sensitivity | | |
| [mV/fC] | $t_p=200$ ns | $t_p=400$ ns | $I_{cm}=12$ nA |
| ENC [e$^-$/rms] | 890 | 860 | 940 |
| Threshold dispersion [e$^-$/rms] | 50 | 45 | 43 |
|         | 45 | 50 | 25 |
transconductor solution, threshold dispersion deserves a more detailed analysis.

**B. Threshold dispersion analysis**

The Apsel MAPS devices were conceived as elementary cells of multichannel detection systems performing high performance parallel processing. In the case of binary front-end chains, like the ones described in this paper, channel-to-channel nonuniformity has to be considered in setting the discriminator threshold for best trade-off between detection efficiency and noise occupancy. The overall effect of such a nonuniformity is usually referred to as threshold dispersion, as it can be conveniently represented in terms of a statistical distribution of the discriminator threshold voltage. In the following theoretical analysis, aiming at comparing the threshold dispersion performances of the two solutions proposed above for the Apsel shaping stage, the contribution from the discriminator will not be considered, as it is the same in the two cases under examination [14].

As far as CMOS processes are concerned, differences in the device threshold voltage $V_{th}$ and in the current gain factor $\beta$ are the predominant mismatch sources in closely spaced, identical-by-design MOS transistors [16]. However, under common operating conditions [17], and all the more so for devices operated close to or in weak inversion (as is the case in the circuits under analysis) [18], effects from $\beta$ mismatch can be safely neglected. In the widely accepted model of $V_{th}$ mismatch [19], the variation in the MOSFET threshold voltage $\Delta V_{th}$ has a normal distribution with zero mean and a variance $\sigma^2(\Delta V_{th})$ inversely proportional to the device gate area:

$$\sigma^2(\Delta V_{th}) = \frac{A_{vth,i}^2}{W/L}, \quad i = n, p.$$  \hspace{1cm} (4)

In (4), $A_{vth,i}$ is a proportionality constant obtained from the characterization of a statistically significant number of device pairs. It is generally provided by the foundry together with the device models and depends on the transistor polarity (indicated through the subscript $n$ or $p$). The main contributions to threshold dispersion are shown in Fig. 2. They come from channel-to-channel mismatch in the input offset of the shaper gain stage, $\Delta V_{thin,s}$, and from device mismatch in the transconductor, represented by the voltage sources $\Delta V_{thp,s}$ and $\Delta V_{thn,s}$. $\Delta V_{thin,s}$ depends on the details of the shaper design; however, it can be considered as chiefly contributed by the shaper input device. No contribution is expected from the charge preamplifier, which is AC coupled to the subsequent blocks. In the case of the Apsel front-end circuit with RC-CR shaper, threshold dispersion has already been studied in detail [14]. Under the hypothesis of small mismatch values, small signal analysis of the circuit yields the following expression for the threshold dispersion:

$$\sigma(V_{t,tr}) = \sqrt{\sigma^2(\Delta V_{thn,s}) + \frac{g_{mp}}{g_{mn}} \sigma^2(\Delta V_{thp,s})}.$$  \hspace{1cm} (5)

In (5), $V_{t,tr} = V_{tr,DC} - V_{t0}$, where $V_{tr,DC}$, the shaper output DC level for the RC-CR shaper case, features random variations from one channel to the other due to the above mentioned threshold dispersion contributions, while $\sigma(V_{t,tr})$ is the standard deviation of $V_{t,tr}$ and $g_{mp}$ and $g_{mn}$ are the channel transconductances of PMOS and NMOS devices respectively in the transconductor. Note that, since $I_I$ is of the order of a few nA, transistors of both polarities in the transconductor are operated in deep subthreshold, therefore resulting in a $\frac{g_{mp}}{g_{mn}}$ ratio slightly smaller than 1. Furthermore, the baseline level at the shaper output, which, assuming perfectly matched N and PMOS devices in the transconductor, is set to $V_{th}$ (the reference transconductor voltage) as an effect of the negative feedback loop, is decoupled from the DC input value and is insensitive to the input offset $\Delta V_{thn,s}$. Therefore, in the first approximation, $\Delta V_{thn,s}$ does not contribute to the overall threshold dispersion. This is not the case in the current mirror shaper, where the output DC level equals the input level again due to the negative feedback loop. The threshold dispersion $\sigma(V_{t,cm})$ for the current mirror configuration is given by

$$\sigma(V_{t,cm}) = \sigma(\Delta V_{thn,s}),$$ \hspace{1cm} (6)

where $V_{t,cm} = V_{cm,DC} - V_{t0}$, $V_{cm,DC}$ being the DC level at the shaper output, randomly varying from channel to channel, in the current mirror case and $\sigma(V_{t,cm})$ is the standard deviation of $V_{t,cm}$. Since reduction in threshold dispersion can only be achieved by increasing the $W \times L$ product, a comparison between (5) and (6) suggests that the current mirror configuration may provide the best compromise between threshold dispersion performance and silicon area occupancy for front-end integration. However, it is worth observing that, since transistors in the transconductor pairs are generally integrated close to each other, the relevant mismatch may be supposed to be smaller than channel-to-channel change in the shaper input offset.

**IV. DNW MAPS WITH SHAPERLESS ANALOG FRONT-END**

The design of a second series of MAPS prototypes, called SDR0 and developed in the framework of the Italian P-ILC experiment, was tailored to vertexing applications at the ILC. In the SDR0 chip, whose layout is shown in Fig. 5, the pixel level front-end processor, was entirely integrated in a 25 $\mu$m x 25 $\mu$m area. The block diagram of the analog processor is shown in Fig. 6. It includes a charge sensitive amplifier, based on a folded cascode gain stage, and a threshold discriminator and can be seen a modified, shaperless version of the analog channel which was integrated in the Apsel series test circuits. The change was forced by the ILC vertex detector point resolution requirements, which, in the case of a binary readout channel, directly impact on the elementary cell dimensions and limits the available area for circuit integration. The DNW detector capacitance is about 140 fF. The preamplifier input NMOS device features a W/L=22/0.25 aspect ratio and a drain current of 1 $\mu$A. Charge restoration in the preamplifier feedback network is obtained through a PMOS current mirror stage, providing a linear discharge of the capacitor $C_{F2}$. The MOM (metal-oxide-metal) feedback capacitance is about 1.3 fF. In order to reduce
high frequency noise effects, the charge preamplifier bandwidth has been purposely limited by capacitively loading (with a capacitance $C_z \simeq 50 \text{ fF}$) its high impedance node. Sparsified readout is achieved by means of a token passing scheme, similar to the one developed for the FPIX2 chip [5], [20]. The prototype MAPS integrated in the SDR0 chips was also carefully designed to meet the severe power dissipation constraints of the ILC vertex detector. A power consumption of about 5 $\mu$W was obtained for the analog front-end channel, which, together with power cycling operation at a 1% duty cycle, makes the overall dissipation compatible with the ILC power specifications.

The measurement scheme used for the characterization of the SDR0 test structures is quite analogous to the one used in the case of the Apsel front-end circuits. The response of the charge preamplifier to a 750 electron charge pulse is shown in Fig. 7. The waveform was measured for different values of the $V_{fb}$ voltage controlling the feedback discharge current through the mirror structure. The peaking time is of the order of 1 $\mu$s. Charge sensitivity characterization was performed, as in the case of the Apsel series MAPS, by measuring the spectral response to $^{55}$Fe. An average value of about 650 mV/fC was found at $V_{fb}$=0, with a 3% dispersion. The measured ENC at the analog output is about 50 electrons, while the threshold dispersion, evaluated by means of threshold scan techniques, is of the order of 60 electrons. Post layout simulations were found to underestimate both noise and threshold dispersion values in the SDR0 prototype. As far as ENC is concerned, this is likely to be due to poor modeling of the DNW capacitance, which was expected to be about 100 fF, and of flicker noise. Discrepancies between simulated and measured threshold dispersion can be ascribed partly to a smaller than expected charge sensitivity, partly to fit errors in extracting the threshold from threshold scan measurements.

V. DESIGN CRITERIA FOR SHAPERLESS ANALOG PROCESSORS

Optimum design criteria for time invariant, classical readout chains processing the signals from capacitive detectors have been extensively discussed in the literature [21]. However, to the best of authors’ knowledge, the case of shaperless analog channels, like the one integrated in the SDR0 prototype, simply consisting of a suitably band limited charge preamplifier, has never been treated in detail. In the following, two different criteria for optimum design of the input transistor in shaperless processors are proposed and discussed. The first one, based on ENC minimization, is suitable for those cases where the effects of the dispersion in the preamplifier output baseline can be strongly attenuated or eliminated (for instance through correlated double sampling techniques or by capacitively decoupling the amplifier from the discriminator). The second criterion, more strictly related to the SDR0 architecture, relies upon the maximization of detection efficiency in multichannel systems with binary readout under noise hit rate constraints. In this
second case, noise and threshold dispersion, both depending on the preamplifier input device dimensions, cannot be optimized separately at the same time. Nevertheless, the optimum discriminator threshold, which is a linear combination of the two contributions, can be minimized to maximize the detection efficiency, therefore providing a different design guideline for the charge preamplifier.

A. Minimum noise design criterion

The first proposed design criterion is based on minimization of the equivalent noise charge. Noise calculations will be performed under the simplifying hypothesis that the current mirror feed-forward network can be modeled by means of a resistor $R_F$. This model can be reasonably adopted as far as small signal analysis is concerned but may be considered quite a crude assumption when large signals are taken into account. If a single pole open loop transfer function, with DC gain $G_D$ and cutoff frequency $f_{0,p}$, is assumed for the charge preamplifier, then the transfer function between the delta-shaped current source at the preamplifier input, modeling the detector response and delivering a charge $Q$, and the preamplifier output $v_{out}$ is given by

$$v_{out} \simeq \frac{GBP}{Q} \cdot \frac{1}{s^2 + s \cdot GBP \cdot \frac{C_{F2}}{GBP} + GBP \cdot \frac{1}{C_T R_F}}.$$  

In (7), $GBP = 2 \pi G_0 f_{0,p} = \frac{g_m}{C_T}$, $g_m$ being the channel transconductance of the preamplifier input device, and $C_T(W) = C_D + C_{in}(W) + C_{F2} \simeq C_D + C_{in}(W)$, where $C_{in}(W) = \frac{3}{2} C_{OX} W L$ is the input capacitance of the charge preamplifier, $C_{OX}$ ($\simeq 14.8$ fF/µm² in STM 130 nm process) is the specific gate oxide capacitance of the preamplifier input device and $W$ and $L$ its channel width and length respectively. More complex and accurate models for the preamplifier input capacitance have been proposed and discussed in the literature, together with their impact on noise minimization in classical readout chains for capacitive detectors [21]. However, the adopted $C_{in}$ model adequately serves the purpose of illustrating, in what follows, the proposed noise minimization procedure for shaperless processors. It can be shown that, if $GBP \cdot C_{F2}^2 \cdot R_F \gg 4 C_T$ is assumed, then (7) can be rewritten as

$$\frac{V_{out}}{Q} \simeq \frac{1}{C_{F2}^2} \left( \frac{1}{s + \tau_1} - \frac{1}{s + \tau_2} \right),$$  

by means of simple fraction expansion. In (8), $\tau_1 = R_F C_{F2}$ and $\tau_2 \simeq \frac{C_T}{GBP \cdot C_{F2}}$. The Laplace antitransform $v_{out}(t)$ of $V_{out}(s)$ can be written as

$$\mathcal{L}^{-1}[V_{out}(s), t] = v_{out}(t) = \frac{Q}{C_{F2}} \left( e^{-\frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}} \right).$$  

It can be easily shown that $v_{out}(t)$ attains a maximum for

$$t = t_p \simeq \frac{C_T}{GBP \cdot C_{F2}} \ln \left( \frac{GBP \cdot C_{F2}^2 R_F}{C_T} \right).$$  

By replacing $t$ with $t_p$ in (9), the peak value $v_{peak}$ of the signal at the charge preamplifier output can be found,

$$v_{peak} = \frac{Q}{C_{F2}^2} \cdot (u^- - u^+), \quad u = \frac{C_T}{GBP \cdot C_{F2}^2 \cdot R_F},$$  

which tends to $\frac{Q}{C_{F2}^2}$ as $R_F \to +\infty$.

In the case of charge measuring systems, the noise properties of the front-end processor are expressed by means of the equivalent noise charge. As a general consideration, the best a designer can do, from the standpoint of noise, when designing a charge preamplifier, is to make all the noise sources in the circuit negligible with respect to the input device contribution. The necessary steps to achieve this result of course depend on the adopted architecture. In the case of a complementary cascode scheme, like the one used in the shaperless amplifier, particular care has to be taken in biasing the current source in the input branch and the cascode PMOS device and choosing their dimensions. Therefore, once the above design measures have been adopted, the preamplifier input device can be safely considered the only source of noise in the front-end. This will be assumed in the foregoing analysis. Fluctuations in the drain current of the input element may be modeled by a voltage source $e_n$ in series with its gate, whose power spectral density includes a channel thermal noise term and a 1/f noise term:

$$\frac{de_n^2}{df} = \frac{4 k_B T}{g_m} + \frac{K_f}{C_{OX} W L f^{\alpha_f}}.$$  

In (12), $k_B$ is the Boltzmann’s constant, $T$ is the absolute temperature, $K_f (\simeq 7 \times 10^{-25}$ J Hz$^{-1}$) in STM 130 nm NMOS, is a 1/f noise intrinsic coefficient and $\alpha_f$ accounts for the slope of the 1/f noise portion of the spectrum. $\Gamma$, the channel thermal noise coefficient, and $g_m$ can both be expressed as a function of $W$ [7]:

$$g_m(W) = \frac{I_D}{n \phi_t} \left[ 1 + \frac{2}{\sqrt{1 + 4 I_D L / T_w}} \right],$$  

$$\Gamma(W) = \frac{1}{1 + I_D L / T_w} \left[ \frac{2}{3} I_D L + \frac{2}{3} T_w \right].$$  

In the previous equations, $I_D$ is the drain current, $n (\simeq 1.2$ in STM 130 nm devices) is the reciprocal of the slope of the $I_D - V_{GS}$ characteristic in the transistor subthreshold region, $\phi_t$ is the thermal voltage and $I_D^* (\simeq 6 \times 10^{-7}$ A in STM 130 nm NMOS transistors) is the normalized drain current marking the boundary between weak and strong inversion [16]. The transfer function between the noise source $e_n$ and the preamplifier output node can be written as

$$\frac{v_{out}}{e_n} \simeq \frac{C_T}{C_{F2}} \frac{1}{1 + s \frac{GBP \cdot C_{F2}}{C_T}},$$  

for a sufficiently large value of $R_F$. The latter assumption is supported by circuit simulations, yielding a small signal resistance of several $\Omega$ for the current mirror in the preamplifier.
feedback network. Taking into account the above results, the equivalent noise charge [22] can be expressed in terms of a thermal noise related and a 1/f noise related contribution,

\[ ENC_{sl}^2(W) = ENC_{sl,th}^2(W) + ENC_{sl,f}^2(W), \]  

where

\[ ENC_{sl,th}^2(W) = k_B T (W) \frac{C_{F2}}{C_z(W)} (C_D + \frac{2}{3} C_OX W L), \]

\[ ENC_{sl,f}^2(W) = \frac{K_f}{C_OX WL} (C_D + \frac{2}{3} C_OX W L)^{\alpha_f + 1} \cdot \left[ \frac{C_{F2} \cdot g_m(W)}{2\pi C_z(W)} \right]^{1-\alpha_f} A_{sl}(\alpha_f). \]

In (17) and (18), the preamplifier charge sensitivity has been approximated to \( C_{F2}^{-1} \). In (18), \( C_z \), already mentioned in section IV, is the capacitance loading the amplifier high impedance node to purposely limit its bandwidth, while \( A_{sl}(\alpha_f) \) is a 1/f noise shaping coefficient, whose value can be calculated as

\[ A_{sl}(\alpha_f) = \int_0^{+\infty} \frac{1}{(1 + x^2)x^{\alpha_f}} dx. \]

Integral (19) converges for \( |\alpha_f| < 1 \). In NMOS transistors, like the preamplifier input device, \( \alpha_f \) is generally smaller than 1. In particular, in the STMicroelectronics 130 nm CMOS process used for the DNW MAPS sensors, \( \alpha_f \approx 0.85 \) [7].

Based on (16), Fig. 8 shows the equivalent noise charge computed as a function of \( W \) for \( I_D = 1 \mu A \) in the preamplifier input device and for \( t_p = 500 \) ns, \( L = 250 \) nm and different values of the detector capacitance \( C_D \). Note that for large values of the input device channel width, differences among the ENC curves tend to disappear. This is due to the fact that for large \( W \) values, the preamplifier input capacitance tends to dominate over the detector capacitance, whose effect becomes negligible. Fig. 8 also shows the individual contributions from channel thermal noise and 1/f noise for \( C_D = 100 \) fF. Very similar considerations apply to Fig. 9, showing the equivalent noise charge as a function of \( W \) for \( I_D = 10 \mu A \) and again for \( t_p = 500 \) ns, \( L = 250 \) nm and for different values of \( C_D \), together with channel width values minimizing the ENC. Here and in the previous figure, the peaking time (see
main noise source, but also provides the main contribution to the threshold dispersion properties of the system. Contributions from the discriminator, which can be managed independently of the preamplifier design and cannot be made negligible by acting on the device dimensions, will not be considered here. It can be easily demonstrated that the effects of the random variation in the preamplifier input offset, represented in Fig. 6 by the voltage source $\Delta V_{\text{th, } p}$ (topologically equivalent to the noise source $e_n$), can be referred to the preamplifier input as

$$\sigma(Q_t) = C_{F2} \cdot \sigma(\Delta V_{\text{th, } p}) = C_{F2} \cdot \sigma(V_{t, sl}) = \frac{C_{F2} A_{\text{th, } n}}{\sqrt{W L}}. \tag{21}$$

In (21), $V_{t, sl} = V_{sl, DC} - V_{t0, sl}$, where $V_{sl, DC}$ is the preamplifier output DC level featuring random variations induced by channel-to-channel differences in the preamplifier input offset and $\sigma(V_{t, sl})$ is the standard deviation of $V_{t, sl}$. $V_{t, sl}$ has been referred to the preamplifier input as $Q_t = C_{F2} \cdot V_{t, sl}$, again taking the preamplifier charge sensitivity to be exactly $C_{F2}^{-1}$. The optimization procedure which was discussed in the previous section based on a noise minimization criterion does not take into any account the way the input device dimensions affect the threshold dispersion properties of the preamplifier. Actually, in a multichannel, binary system, both noise and threshold dispersion characteristics have to be considered in order to determine the discriminator threshold which optimizes detection efficiency. Optimum efficiency is generally constrained by the maximum rate of noise induced transitions at the discriminator output, or maximum noise hit rate, $f_{n, \text{max}}$, due to the signal at the preamplifier output randomly crossing the discriminator threshold. Such a noise hit rate limit is strongly dependent on the readout architecture and on the target readout efficiency. Under some very general assumptions, in a binary channel the noise hit rate $f_{n0}$, whose analysis represents a specific aspect of the more general level crossing problem, can be written as [25]

$$f_{n} = f_{n0} \cdot e^{-\frac{Q_{t0}^2}{2 \cdot \text{ENC}_{sl}}}, \tag{22}$$

where $Q_{t0}$ is the mean value of the random variable $Q_t$ and $f_{n0}$ is the noise hit rate at zero threshold, i.e. at $Q_t = 0$. For any given peaking time, $f_{n0}$ can be shown to be virtually independent of $W$, $L$, $I_D$ and $C_D$. If we neglect the effect of threshold dispersion, the minimum input referred discriminator threshold $Q_{t, \text{min}}$ may be set, for all the channels, based on the maximum noise hit rate $f_{n, \text{max}}$ the system can afford and on the ENC performance of the charge preamplifier:

$$Q_{t, \text{min}} = \sqrt{2 \cdot \ln \left( \frac{f_{n0}}{f_{n, \text{max}}} \right)} = \rho(f_n) \cdot \text{ENC}_{sl}, \tag{23}$$

where $\rho(f_n) = \sqrt{2 \cdot \ln \left( \frac{f_{n0}}{f_n} \right)}$ is an extremely slowly increasing function of the ratio between the zero threshold noise hit rate $f_{n0}$ and the system maximum noise hit rate $f_{n, \text{max}}$. 

**B. Design for optimum detection efficiency**

In the shaperless processor of the ILC-class DNW MAPS, the input device of the charge preamplifier not only accounts for the
rate and the noise hit rate, varying from about 3 to about 4.8 for $\frac{L}{t_p}$ ranging from 100 to 100000. Actually, if the threshold is set according to (23), due to threshold dispersion, a significant fraction of the channels could exceed the maximum admissible noise hit rate $f_{n,max}$ (see Fig. 12). Therefore, $Q_{t,min}$ should be suitably changed to take into account threshold dispersion effects:

$$Q_{t,min} = \rho \cdot ENC_{sl} + \lambda \cdot \sigma(Q_t).$$  \hspace{1cm} (24)$$

For instance, let us assume that $Q_t$ features a normal distribution with mean value $Q_{t0}$ (the externally set threshold) and standard deviation $\sigma(Q_t)$. If $\lambda = 0$, then half the channels will find themselves exceeding the maximum noise hit frequency (see again Fig. 12). In order to keep 98% of the channels above the minimum tolerable threshold, $\lambda \approx 2$ should be chosen. As a matter of fact, with such a choice of $\lambda$, the fraction of hot channels $n_{hc}$, i.e. channels not complying with the maximum noise hit rate constraint, is found to be

$$n_{hc}(\lambda = 2) = \frac{1}{2} \left[ 1 - Erf \left( \frac{\lambda}{\sqrt{2}} \right) \right]_{\lambda = 2} \simeq 0.02275$$  \hspace{1cm} (25)$$

where $Erf(x)$ is the error function. For the purpose of emphasizing the dependence of $Q_{t,min}$ on the channel width of the preamplifier input device, (24) can be rewritten as

$$Q_{t,min}(W) = \rho(f_{n,max}) \cdot ENC_{sl}(W) + \lambda(n_{ch,max}) \cdot C_F A_{eth,n} \frac{1}{\sqrt{W \cdot L}},$$  \hspace{1cm} (26)$$

where $\rho$ and $\lambda$ have been written as functions, respectively, of the maximum admissible noise hit rate, $f_{n,max}$, and of the maximum number of hot channels, $n_{ch,max}$, to emphasize the driving criteria for their choice. Fig. 13 shows the input referred discriminator threshold as a function of the channel width of the preamplifier input device for $L = 250$ nm, $I_D = 1$ $\mu$A, $t_p = 500$ ns, $\rho = 4$ and $\lambda = 2$ and for different values of the detector capacitance $C_D$. In Fig. 14 the curves have been plotted for $I_D = 10$ $\mu$A and for the same values of $C_D$ as in Fig. 13. In the same figures, the values of $W$ minimizing $Q_{t,min}$ are also shown. Change in the optimum $W$ in Fig. 14 with respect to Fig. 13 is to be ascribed to the decrease in the channel thermal noise contribution with the drain current observed in Fig. 11. It is worth noting that the obtained optimum channel widths are significantly larger than the values provided by the minimum noise criterion for the same detector capacitances and input device drain currents.

C. ROC graph analysis

A deeper, though qualitative, insight into the effects of threshold dispersion on optimum threshold setting can be
gained through receiver operating curve (ROC) analysis [26].

ROC graphs have in particular been used in signal detection theory to assess the performance of classification models, or classifiers, in terms of a trade-off between signal hit rates (or true positives, TP) and false alarm rates (or false positives, FP). An analog processor behaves as a probabilistic classifier in that the peak value of its response to an input signal, either being the result of a particle passing through the detector or of a noise hit, represents the input signal probability of belonging to one of two classes, i.e. signal or noise. Such a probabilistic classifier can be used with a threshold to produce a binary classifier, yielding a point in the ROC space for each threshold value. For the threshold ranging from $-\infty$ to $+\infty$, a curve is traced through ROC space. A multichannel binary system can itself be treated as a binary classifier. If each channel features the same probability density function (PDF) for the charge collected by the detector and the same equivalent noise charge, then, assuming no threshold dispersion, the multichannel system behavior as a binary classifier cannot be told from that of its single members. Things change when threshold dispersion comes into play. It might actually be interesting to evaluate how threshold dispersion affects the ROC graph in a set of binary detectors. For the sake of example, let us consider the curves in Fig. 15, representing the probability density functions of the signal, the noise and the threshold (the latter shown in three different versions with varying standard deviation) for a multichannel system. The Moyal’s PDF $\Psi(Q)$ [27], emulating the Landau distribution of charge in thin absorbers, is assumed for the signal distribution

$$\Psi(Q) = \frac{\sqrt{\frac{2}{\pi}} e^{-\frac{(Q-Q_{sl})^2}{2Q_{sl}^2}}}{\sqrt{2\pi Q_{sl}^2}}.$$  \hfill (27)

where $Q_{sl}=400$ electrons is a constant depending on the absorber and $Q_{sl}=1000$ electrons is the most probable value of the detected charge. For both the noise and the threshold distributions, $N(Q)$ and $Th(Q)$ a Gaussian function is assumed:

$$N(Q) = \frac{1}{ENC_{sl}\sqrt{2\pi}} e^{-\frac{Q^2}{2ENC_{sl}^2}}, \quad (28)$$

$$Th(Q, Q_{sl}) = \frac{1}{\sigma(Q_{sl})\sqrt{2\pi}} e^{-\frac{(Q-Q_{sl})^2}{2\sigma(Q_{sl})^2}}, \quad (29)$$

where $ENC_{sl}=50$ electrons, $Q_{sl}=200$ electrons and $\sigma(Q_{sl})$ is made to assume three different values, 50, 100 and 200 electrons. Note that $Th(Q, Q_{sl})$ collapses into a Dirac mass, $\delta(Q - Q_{sl})$, as $\sigma(Q_{sl}) \to 0$. The ROC curves can be traced as parametric plots with the FP rate, $FP'$, and the TP rate, $TP'$, as the $x$ and $y$ coordinates and the externally set threshold $Q_{sl}$ as the parameter. $FP'$, the rate of noise hits mistaken for signals ($\frac{\text{negatives incorrectly classified}}{\text{total negatives}}$), and $TP'$, the rate of signals recognized as such ($\frac{\text{positives correctly classified}}{\text{total positives}}$), can be calculated as follows:

$$FP'(Q_{sl}) = \int_{-\infty}^{+\infty} Th(u, Q_{sl}) \int_{Q_{sl}}^{+\infty} N(v)dvdu, \quad (30)$$

$$TP'(Q_{sl}) = \int_{-\infty}^{+\infty} Th(u, Q_{sl}) \int_{u}^{+\infty} \Psi(v)dvdu. \quad (31)$$

The resulting ROC curves are shown in Fig. 16. In particular, the upper left corner of the graph has been emphasized for the purpose of stressing the modifications induced by changes in the threshold dispersion value. A couple of considerations are in order. First of all, for increasing values of $\sigma(Q_{sl})$, an apparent performance degradation of the system seen as a binary classifier can be detected. For a given $FP'$ coordinate, the corresponding $TP'$ coordinate on ROC curves gets larger as the threshold dispersion gets smaller. Second, for a given mean threshold value $Q_{sl}$ (which corresponds, it is worth repeating, to the value of the threshold as it is globally set for the multichannel system), the corresponding false positive rate coordinate increases with increasing $\sigma(Q_{sl})$. This is in agreement,
at least qualitatively, with the increase of the fraction of hot channels due to threshold dispersion discussed in Section V-B. Increasing the threshold value, for instance from 200 to 300 electrons on the characteristic obtained at $\sigma(Q_t) = 200$ e$^{-}$, as shown in Fig. 16, shifts the point on the ROC curve towards smaller false positive rates, at the expense of the true positive rate.

VI. RC-CR SHAPING VERSUS SHAPERLESS OPERATION

In section IV, the shaperless processor has been presented as a possible alternative to classical optimum readout chains with bandpass filtering in the case of DNW MAPS featuring a small pitch, of the order of 20 μm. In this last section, a comparison between the shaperless and the RC-CR shaper solutions is proposed from the standpoint of noise and threshold dispersion.

A. Noise analysis

It seems quite reasonable to expect that eliminating the shaping stage may lead to noise performance degradation, particularly as far as the low frequency contributions are concerned. In a front-end channel with a first order semigaussian unipolar bandpass filter, the ENC can be expressed as [7],

$$ ENC_{bp}(W) = ENC_{bp,th}(W) + ENC_{bp,f}(W), $$  \hfill (32)

where the first and the second terms arise respectively from the channel thermal noise and the flicker noise contributed by the preamplifier input device (supposed to feature the same noise power spectral density as given by (12)):

$$ ENC_{bp,th}^2(W) = C_T(W)^2 \cdot \frac{4k_BTT(W)}{g_m(W)} \cdot \frac{A_1}{t_p}, $$  \hfill (33)

$$ ENC_{bp,f}^2(W) = C_T(W)^2 \cdot \frac{(2\pi)^{\alpha_f}}{\Omega} \cdot \frac{A_2(\alpha_f)}{C_{ox}W}. $$  \hfill (34)

In the previous equations, where $A_1 = 0.92$ and $A_2 = 0.85$ are RC-CR shaping coefficients [7], the ENC dependence on $W$ has been emphasized. For the case of the ENC in a shaperless front-end channel, (16), (17) and (18) apply. However, for the sake of comparison, it may be useful to replace $C_z$ in (17) and (18) with its expression given by (20). This yields

$$ ENC_{sl,th}^2(W) = \frac{[\Omega(-1, -t_p)}{2A_1} \cdot ENC_{bp,th}^2(W), $$  \hfill (35)

$$ ENC_{sl,f}^2(W) = \frac{A_{sl}(\alpha_f)}{2\pi A_2(\alpha_f)} \cdot ENC_{bp,f}(W). $$  \hfill (36)

where, it is worth noting, the factors multiplying $ENC_{bp,th}^2(W)$ and $ENC_{bp,f}(W)$ are independent of $W$. Fig. 17 shows the equivalent noise charge for a shaperless processor and for a processor featuring RC-CR filtering as a function of $W$ for four different values of the detector capacitance and for $L = 250$ nm, $I_D = 1$ μA and $t_p = 500$ ns. Advantage of semigaussian shaping is most prominent at small channel width values, where the contribution from 1/f noise is predominant for the shaperless channel. At larger $W$ values, where channel thermal noise contribution becomes the most important, the ENC tends to become independent of the adopted solution, although a slight advantage is maintained by the channel with RC-CR shaping. In Fig. 18, the equivalent noise charge is plotted as a function of $W$ again for a shaperless processor and for a processor featuring RC-CR shaping. The curves have been obtained for different values of the peaking time and for $L = 250$ nm, $I_D = 1$ μA and $C_D = 200$ fF. Very similar considerations as for Fig. 17 applies to Fig. 18. The advantage of RC-CR shaping is conspicuous at small values of the input device channel length and becomes less sizeable at larger $W$ values. Moreover, again for large input device channel widths, at a given $t_p$, the larger the peaking time value, the smaller the difference between the ENC curves featured by the two
solutions under analysis.

As a final consideration, use of a bandpass filtering stage in the analog front-end is, not surprisingly, advisable as it provides low frequency noise rejection. As a consequence, optimum ENC value in analog channels with RC-CR shaping, at a given peaking time and a given detector capacitance, is always smaller than in the case of a shaperless processor. Moreover, in the case of RC-CR shaping (the same applies to all kind of bandpass filtering, where the charge preamplifier is AC coupled to the shaper), the noise optimization problem is decoupled from threshold dispersion minimization. However it is worth observing here that, in the particular case of the DNW MAPS treated in this work, the detector capacitance increases with the complexity of the analog front-end electronics, whose NMOS parts are integrated inside the deep N-well sensor, therefore determining its area. The difference in sensor area between the two considered cases may be (and indeed is in the circuits discussed in the first part of this work, compare noise experimental data in sections III and IV) such that the noise performance discrepancy is almost completely eliminated.

B. Threshold dispersion analysis

In both the shaperless and the RC-CR solutions, a non negligible contribution to the threshold dispersion properties comes from the threshold discriminator. This common contribution will be neglected in the following discussion to focus on the distinctive features of the two stages. The input referred threshold dispersion for the shaperless preamplifier, already calculated in Section V-B, is provided by (21). In the case of the front-end channel with RC-CR shaping stage, the input referred threshold dispersion is given by

\[
\sigma_{tr}(Q_t) = \frac{eC_2C_{F1}}{2C_1} \sqrt{\frac{A_{vth,n}^2}{W_n L_n} + \frac{g_{mp}^2 A_{vth,p}^2}{g_{mn}^2 W_p L_p}}
\]

\[
\approx \frac{eC_2C_{F1}}{2C_1} \cdot \frac{A_{vth,n}}{W_n^{1/2} L_n^{1/2}}.
\]

For the sake of simplicity, in (37), \(\sigma_{tr}(Q_t)\), where the subscript \(n\) refers to the NMOS device in the transconductor differential pair and the subscript \(p\) refers to the PMOS devices in the transconductor mirror load, the contribution from P-type transistors has been dropped taking into account the actual values of the device parameters and dimensions in the circuit. The ratio between the input referred contributions in the shaperless and RC-CR amplifiers is

\[
\frac{\sigma_{stl}(Q_t)}{\sigma_{tr}(Q_t)} = \frac{2C_1 C_{F2}}{eC_2 C_{F1}} \sqrt{\frac{W_n L_n}{W L}}.
\]

Some very qualitative considerations apply to (38). The factor corresponds to the ratio between the charge sensitivity of the RC-CR amplifier and that of the shaperless stage. Its value is expected to be slightly larger than 1. As a matter of fact, while the overall charge sensitivity in the RC-CR front-end is attained through the cascade of two gain stages, a single gain stage is available in the shaperless solution. Here, for stability and reproducibility reasons, the value of the feedback capacitance cannot be chosen to be as small as needed for the charge sensitivity to equal the RC-CR amplifier gain. The second term in (38), the square root of the ratio between the area of the NMOS device in the transconductor differential pair (generally featuring a few micron value for both width and length) and that of the shaperless amplifier input device (generally featuring large \(W\) and deep submicron \(L\)), may slightly vary around unity. It is worth recalling here that, as discussed in Section V, the dimensions of the shaperless stage input NMOS may be bound by optimum detection efficiency or noise minimization constraints. Also, due to the smaller pitch, room for the discriminator layout may be smaller in the case of the shaperless amplifier than for the RC-CR processor. Therefore, in conclusion, the latter may offer better threshold dispersion performances.

VII. CONCLUSION

In this paper, two different analog processors for deep N-well MAPS fabricated in a 130 nm CMOS process by STMicroelectronics have been presented. The circuits have been designed under the severe constraint set by the point resolution requirements of vertexing applications at the SuperB Factory and at the International Linear Collider. In the case of the Apsel MAPS, developed for applications to the SuperB vertex detector, use of a shaping stage with current mirror feedback network proved particularly effective from the standpoint of threshold dispersion. In the case of the monolithic sensor for applications to the ILC vertex detector, integrated in the SDR0 chip, a more compact, shaperless design has been proposed for the analog readout electronics. Since, in this circuit, the input device is the main source both of noise and threshold dispersion, a new criterion for optimum design could be defined, targeting maximization of detection efficiency in multichannel systems under noise hit rate constraints. The two proposed analog processors and their variants have been fully characterized. The experimental results are very encouraging and confirm the degree of maturity reached by CMOS DNW MAPS design. However, in order to fully comply with the specifications of experiments at the SuperB Factory and at the ILC, device performances still need to be improved. Both in the case of the Apsel and the SDR0 chip, use of vertical integration (so called 3D) technologies may help increase the functional density of the front-end circuits and enhance their properties by placing the digital section in a different layer from the one used for the collecting electrode. For this purpose, new versions of the Apsel and SDR0 chips are being designed under the severe constraint set by the point resolution requirements of vertexing applications at the SuperB Factory and at the International Linear Collider.
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