Front-end performance and charge collection properties of heavily irradiated DNW MAPS

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Abstract—Deep N-well (DNW) CMOS monolithic active pixel sensors (MAPS) fabricated in a 130 nm technology have been exposed to γ-rays up to an integrated dose of about 10 Mrad and subjected to a 100 °C/168 h annealing cycle. Device tolerance to total ionizing dose has been evaluated by monitoring the charge in charge sensitivity, noise and charge collection properties after each step of the irradiation and annealing campaign. Damage mechanisms and their relation to front-end architecture and sensor features are thoroughly discussed by comparing the response to ionizing radiation of different test structures and based on radiation induced degradation models in single MOS transistors.

Index Terms—MAPS, deep N-well, ionizing radiation, CMOS, analog front-end.

I. INTRODUCTION

DEEP N-well (DNW) CMOS monolithic active pixel sensors (MAPS) were proposed a few years ago to enable the design of large, highly granular matrices of thin charged particle detectors with fast readout architecture based on sparsification techniques [1]. The DNW MAPS approach takes advantage of the properties of triple well structures to lay out a sensor with relatively large area (as compared to standard three transistor MAPS [2]) read out by a classical processing chain for capacitive detectors. The sensor, featuring a buried N-type layer with N-wells (NW) on its contour according to a typical deep N-well scheme, collects the charge released by the impinging particle and diffusing through the substrate, whose active volume is restricted to the uppermost 20-30 µm thick layer below the collecting electrode. Therefore, within this extent, substrate thinning is not expected to significantly affect charge collection efficiency, while improving momentum resolution performance in charged particle tracking applications. As mentioned above, DNW MAPS are being developed chiefly to comply with the intense data rates foreseen for tracking applications at the future high energy physics (HEP) facilities. Based on the proposed solution, the MAPS detectors of the Apsel series, which are among the first monolithic sensors with pixel-level data sparsification [3], [4], [5], have been developed and successfully tested at the Proton Synchrotron facility at CERN [6]. Depending on the experimental environment and on the position inside the detector, MAPS sensors will be required to withstand a total ionizing dose (TID) which can range from a few hundreds of krad(SiO₂) [7] to about ten Mrad(SiO₂) [8]. The effects of ionizing radiation on DNW MAPS were discussed for the first time in a previous work [11] which was mainly focused on studying the damage mechanisms in the readout electronics. In that work, the devices under test (DUT) were exposed to a maximum dose of 1.1 Mrad(SiO₂). The present paper is concerned with the effects of higher γ-ray doses, well beyond 1 Mrad(SiO₂) and compatible with vertex detector applications at the SuperB Factory experiment [8]. Furthermore, besides studying the performance of the front-end processor, this work also investigates the charge collection properties of the sensing electrode under heavy irradiation conditions. This has been done by means of measurement techniques involving a laboratory ⁵⁵Fe radiation source and an infrared laser.

II. DUTS AND IRRADIATION AND TEST PROCEDURES

The DUT, called Apsel3T1, was designed and fabricated in a 130 nm CMOS technology and includes a number of structures with different features, described in detail in Table I. In all of the tested devices, the signal coming from the sensor (or from an external pulser through a 30 fF MIM injection capacitor) is processed by means of the readout chain shown in Fig. 1, including a charge preamplifier, an RC-CR shaper, a threshold discriminator and a set-reset bistable circuit acting as a memory cell. The analog front-end performs continuous time charge amplification and shaping, which is a classical choice for capacitive detectors [9]. This has to be contrasted with the typical, imaging-like approach, where correlated double sampling (CDS) techniques are used to perform time-variant filtering. The adopted solution lends itself in a more straightforward way to implementing a data driven readout architecture [10]. In Fig. 1, \( C_F \) is the preamplifier feedback capacitor, continuously reset by means of the \( M_F \) NMOS transistor operated in the deep subthreshold region. Moreover, \( A(s) \) is the transfer function of the shaper gain stage, \( C_1 \) is the differentiating capacitance at the shaper input, while \( G_m \) and \( C_2 \) are the transconductance and the capacitance in the shaper feedback network. By acting on the capacitance in the high impedance node of the shaper gain stage and on the
TABLE I

<table>
<thead>
<tr>
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<th>APSEL3T1 CHIP DESCRIPTION</th>
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<tr>
<td>M1</td>
<td>3×3 matrix, all analog outputs accessible, injection capacitance (C_{inj} = 30 fF) for the central pixel, collecting electrode featuring a main body and satellite N-well diffusions, an area of 670 μm² and a perimeter of 315 μm</td>
</tr>
<tr>
<td>M2</td>
<td>3×3 matrix, all analog outputs accessible, injection capacitance (C_{inj} = 30 fF) for the central pixel, T-shaped collecting electrode featuring an area of 880 μm² and a perimeter of 190 μm</td>
</tr>
<tr>
<td>M3</td>
<td>8×8 matrix, with row by row, 8 parallel digital readout, one cell with injection capacitance (C_{inj} = 30 fF) and analog output accessible (T-shaped collecting electrode area), half the matrix featuring M1-like cells, the other half M2-like cells</td>
</tr>
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III. EFFECTS OF 60Co γ-RAYS ON DNW MAPS PERFORMANCE

The ionizing effects of 60Co γ-rays on DNW MAPS have been studied by analyzing radiation-induced variations in the most significant parameters of the front-end electronics and of the collecting electrode. In the following, a selection of the test results is shown, providing some paradigmatic examples of the DUT behavior.

A. Effects on charge sensitivity

Exposure of the DNW MAPS to ionizing radiation is responsible for a significant decrease in charge sensitivity. This can be observed in Fig. 2, showing the charge sensitivity as a function of the integrated dose for the accessible pixel of an M3 matrix. The data, which also include post-annealing...
measurement results, are plotted for the two available peaking times, 200 and 400 ns. Before irradiation, at each irradiation step (900 krad, 2660 krad and 8200 krad for chips 24 and 25, 900 krad, 3300 krad and 9700 krad for chips 27 and 29) and after annealing, the gain value has been extracted by linearly fitting the peak response of the front-end channel to a voltage step with varying amplitude at the input MIM capacitor $C_{inj}$ (see Fig. 1). The corresponding amount of injected charge has been calculated by taking into account the nominal $C_{inj}$ capacitance, 30 fF. Before irradiation, the charge sensitivity is about 1.5 V/fC at a peaking time $t_p=200$ ns, about 1.3 V/fC at $t_p=400$ ns. The decrease after exposure to a 900 krad(SiO$_2$) γ-ray dose is about 7% at both peaking times. This result is in fair agreement with the outcomes of the rad-hard characterization of the Apsel2T MAPS sensors [11], where the maximum observed change in charge sensitivity, actually after a slightly larger integrated dose (1.1 Mrad(SiO$_2$)), was just over 10%. After irradiation with an integrated dose of 9700 krad(SiO$_2$), the charge sensitivity is found to be slightly more than 80% of its original value at $t_p=200$ ns and slightly less than 75% of the pre-irradiation value at $t_p=400$ ns. The annealing cycle brings the charge sensitivity back to a state not far from its pre-irradiation condition. The mechanisms underlying such a behavior, thoroughly analyzed in the case of the Apsel2T chip [11], are briefly summarized in the following together with new supporting evidence. In particular, charge sensitivity was found to decrease as a result of 1) the threshold voltage shift in the feedback NMOSFET $M_F$ of the charge preamplifier, only partially compensated by 2) the leakage current increase in the detector, and as a consequence of 3) the change in the feedback transconductance and in the gain-bandwidth product of the shaping stage.

1) Threshold voltage shift in $M_F$. Although deep submicron CMOS technologies are acknowledged to possess quite a high degree of radiation tolerance [13], nevertheless, N- and PMOS devices, belonging to the 130 nm CMOS node and featuring a channel width $W$ smaller than about 1 μm, were proven to undergo the so called radiation induced narrow channel (RINC) effect, involving charge trapping in the shallow trench isolation (STI) oxides. This has been proposed as the main cause for a substantial change in the drain leakage current and in the threshold voltage [14]. This phenomenon is likely to affect $M_F$ in the preamplifier feedback network, featuring $W = 0.18 \mu$m and channel length $L = 10 \mu$m. A couple of devices, $NM1$ and $NM2$, belonging to the same technology as the Apsel3T1 and with the same aspect ratio as $M_F$, have been exposed to different integrated doses of γ-rays to search for possible evidence of the RINC effect also in the technology used for the Apsel3T1 MAPS devices. During irradiation they were kept with their source and drain grounded and the gate biased to 1.2 V. This was done for the sake of comparison with the results from rad-hard tests on wider channel devices from the same node and manufacturer and on narrow channel transistors belonging to the same node but coming from a different foundry. Fig. 3 shows the variation in the threshold voltages of $NM1$ and $NM2$. The change is of the order of a few tens of mV, significantly larger than found in transistors with larger $W$ from the same process [13]. Interestingly enough, a partial recovery can be detected for $NM2$ just after the last irradiation step, as a possible consequence of the interface state negative charge starting to compete with the oxide-trapped positive charge (as it was observed in the technology where the RINC effect was recognized for the first time [14]). On the other hand, no hint of such a rebound-effect (not to be confused with annealing-induced recovery) can be found in Fig. 2 (nor in the data presented in the next sections). This may be due to the operating conditions of $NM2$ in Fig. 3 being different from those of $M_F$. Also, the starting TID value for the rebound-effect may vary by several Mrad [14]. It is worth mentioning in conclusion of this section that no thorough study was carried out on possible TID induced formation.

![Fig. 2. Charge sensitivity as a function of the total ionizing dose and after the annealing procedure for the accessible pixel of an M3 matrix. Data are plotted for the two available peaking times.](image)

![Fig. 3. Variation of the threshold voltage in a couple of irradiated narrow channel NMOSFETs.](image)

<table>
<thead>
<tr>
<th>name</th>
<th>area [μm$^2$]</th>
<th>perimeter [μm]</th>
</tr>
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<tbody>
<tr>
<td>A</td>
<td>55 - 10$^3$</td>
<td>1194</td>
</tr>
<tr>
<td>B</td>
<td>16,1 - 10$^3$</td>
<td>638</td>
</tr>
<tr>
<td>C</td>
<td>4 - 10$^4$</td>
<td>318</td>
</tr>
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**TABLE II**

**Geometrical features of the tested octagonal DNW diodes**
Fig. 4. Leakage current as a function of the reverse voltage in a deep N-well diode. The preirradiation curve is compared to the ones obtained after exposure to a 900 krad(SiO₂) and to a 3300 krad(SiO₂) TID.

Fig. 5. Leakage current at a reverse voltage of 5 V as a function of the junction perimeter length after irradiation with a 900 krad(SiO₂) and a 3300 krad(SiO₂) TID for the three test diodes described in Table II.

Fig. 6. Radiation effects on the amplitude and shape of the MAPS response to a 750 electron input charge. The pixel belongs to an M3 matrix.

Fig. 7. Leakage current increase in the detector. Response to ionizing radiation of the DNW detector was studied by testing a set of three octagonal DNW diodes whose geometrical features are listed in Table II (see Table I for a comparison with the area and perimeter of the ApSiel3T1 sensors). Fig. 4 shows the leakage current in an A diode for a reverse voltage spanning from 0 to 10 V at varying TID. A substantial increase can be detected over the entire reverse voltage range. The buildup of holes in the field oxide and the creation of trapping states at the Si/SiO₂ interface over the PN junction may account for an increase of the surface generation current [15], [16]. Based on the involved damage mechanism, the leakage current is supposed to be proportional to the length of the junction at the silicon surface. This is supported by the results shown in Fig. 5, where the leakage current at a reverse voltage of 5 V is plotted as a function of the junction perimeter length after irradiation with a 900 krad(SiO₂) and a 3300 krad(SiO₂) TID for the three test diodes described in Table II. Data points can be fitted fairly well to a linear function, demonstrating that no significant bulk damage effect, which would be roughly linearly dependent on the junction area, contributes to the leakage current increase. This result agrees with the literature data reporting on the relatively small values of the ⁶⁰Co γ-ray bulk damage factor in silicon diodes [17], which, as calculations confirm, yields a completely negligible leakage current term from the depleted volume.

3) Change in the feedback transconductance and in the gain-bandwidth product of the shaper. Also in the shaping filter, the RINC effect provides a further contribution to charge sensitivity decrease. Radiation induced change in the threshold voltage of the PMOS current source (featuring \( W = 0.18 \) μm) in the shaper input stage is responsible for a decrease in the gain-bandwidth product. On the other hand, a threshold voltage shift in the transconductor current sources (all featuring \( W = 0.25 \) μm), may result in an increase of the feedback transconductance. Both effects combine to bring about a reduction in the peak response of the analog channel [11]. Moreover, transconductance increase is expected to speed up the return to the baseline of the shaper response. This is actually confirmed by the waveforms in Fig. 6, illustrating the effects of radiation on the response of a DNW MAPS to an input charge of 750 electrons. Return to baseline grows faster with increasing TID. Note that, after annealing, the pixel response is restored virtually to its original state.

B. Effects on noise performance

Equivalent noise charge (ENC) is a figure of merit for analog processors, defined as the charge to be injected at the input of a charge measuring system to have a peak response as high as the output root mean square noise. In the monolithic sensors under test, the main noise contribution comes from the fluctuations in the drain current of the preamplifier input
device. At the available peaking times, other contributions from the preamplifier feedback network and from the detector leakage current can be safely dropped. This is also supported by the results of the rad hard tests on the Apsel2T chip, where noise contributions other than the one from the input device were found to be negligible at $t_p=500 \text{ ns}$ [11]. The noise in the preamplifier input transistor can be represented by means of a voltage source in series with the device gate. Its power spectral density $S_w^2(f)$ is given by

$$S_c^2 = S_w^2 + A_f \frac{K_f}{WLC_{ox}f^{\alpha_f}}.$$  \hspace{1cm} (1)

with $A_f = \frac{K_f}{WLC_{ox}}$. The previous equation includes a frequency independent component, $S_w^2$, mainly accounting for the channel thermal noise in the input device drain current, and a $1/f$ term, $A_f$. In the equation, $n$ is the subthreshold slope coefficient, $\gamma$ is the channel thermal noise coefficient, depending on the device operating point and polarity, $k_B$ is the Boltzmann’s constant, $T$ is the absolute temperature, $g_m$ is the device transconductance, $K_f$ is an intrinsic $1/f$ noise process parameter, $C_{ox}$ is the gate oxide specific capacitance and $\alpha_f$ is the $1/f$ noise slope coefficient (about 0.85 in the NMOS devices from the 130 nm process used for the tested MAPS [18]). Eq. (1) does not include any Lorentzian term pointing to possible random telegraph signal (RTS) phenomena, which are typically found in small area MOSFETs [19], [20]. Such phenomena were actually detected only in some of the smallest among the irradiated single device samples, featuring W/L=10/0.13. In transistors with gate area of the same order of the preamplifier input device or larger, the low frequency spectrum, both before and after irradiation, was found to be dominated by flicker noise. This is shown as an example in Fig. 7 for an NMOS with W/L=20/0.20 irradiated with a 1.1 Mrad(SiO$_2$) $\gamma$-ray dose. The expected pre-irradiation behavior of the preamplifier input device from the standpoint of the noise voltage spectrum is the total capacitance shunting the charge preamplifier and $C_T$. In the equation, $C_T$ is the total capacitance shunting the charge preamplifier and $A_1$ and $A_2$ are shaping coefficients. The effects of radiation on the ENC are shown in Fig. 9, where the equivalent noise charge is plotted as a function of the absorbed dose and after the annealing cycle for the central pixel of an M1 matrix. ENC is plotted for the two available peaking times.
the peaking time, after exposure to radiation. The annealing procedure brings the noise performance back to somewhere between the starting DUT state and the post-900 krad step condition. It is worth recalling that the charge sensitivity features a qualitatively similar response, with a remarkable performance recovery after annealing, possibly due to partial annihilation of the positive charge trapped in the STI. ENC degradation after irradiation is likely to originate from low frequency noise increase in the preamplifier input device. According to the model validated in previous works [21], [22], flicker noise gets worse as a consequence of parasitic lateral transistors being turned on by positive charge buildup in the shallow trench isolation oxides and contributing to the overall noise. Radiation induced increase in border trap density provides a further, although minor, contribution to the overall noise degradation. The role of STI and parasitic lateral transistors in 1/f noise degradation has been emphasized in deep submicron technologies, in particular in 130 nm and 90 nm ones. It was probably less significant, if not negligible, in older CMOS generations, where the contributions from border trap density increase and charge buildup in the transistor gate oxide were predominant [23], [24]. In irradiated devices, flicker noise increase can be expressed through the ratio between the post-irradiation coefficient \( A_{f,post} \) and its pre-irradiation value \( A_{f,pre} \):

\[
\frac{A_{f,post}}{A_{f,pre}} = \frac{K_{f,m,post}}{K_{f,m,pre}} \left( \frac{1 + \frac{W_{Cox}}{W_{lat,eff}} g_{m,post}^2}{1 + \frac{g_{m,post}}{g_{m,post}^2}} \right)^2.
\]

(3)

In (3), \( K_{f,m,pre} \) is the preirradiation intrinsic process parameter for 1/f noise in the main device, \( K_{f,m,post} \) and \( K_{f,lat} \) are post-irradiation intrinsic process parameters in the main and in the parasitic transistor respectively, \( C_{ox,lat} \) is the effective oxide capacitance of the parasitic STI sidewall transistor, \( g_{m,post} \) is the channel transconductance in the main device and \( g_{m,lat} = 2n_f g_{m,lat,s} \), with \( n_f \) the number of fingers composing the main transistors and \( g_{m,lat,s} \) the transconductance of the single parasitic device. Note that for each finger, two single parasitic devices get switched on by charge trapped in the STI, each with channel length \( L \) and channel width \( W_{lat,s} = \frac{W_{lat}}{2n_f} \). Under the simplifying hypothesis, generally valid in the low power operation adopted for DNW MAPs, that the main and the single parasitic devices are made to work in weak and strong inversion respectively [21], then

\[
g_{m,lat,s} \approx \sqrt{\frac{2\mu_n C_{ox,eff} W_{lat,s}}{L}} I_{D,lat,s}, \quad \text{(4)}
\]

\[
g_{m,m,post} \approx \frac{I_{D,m,post}}{n \phi_t}, \quad \text{(5)}
\]

with \( \mu_n \) the electron mobility in silicon, \( I_{D,lat,s} \) the drain current in the single parasitic transistor, \( I_{D,m,post} \) the post-irradiation drain current in the main device and \( \phi_t \) the thermal voltage. If \( g_{m,lat,s} \gg 1 \) is also assumed, (3) can be rewritten as

\[
\frac{A_{f,post}}{A_{f,pre}} \approx \frac{K_{f,m,post}}{K_{f,m,pre}} \left( 1 + \frac{W_{Cox}}{W_{lat,eff}} g_{m,post}^2 \right)^2,
\]

(6)

where \( I_z^* = 2\mu_n C_{ox} n \phi_t^2 \) is the normalized drain current marking the boundary between weak and strong inversion. Equation (6) points out that, for a given CMOS process, flicker noise degradation is larger in devices with larger number of fingers \( n_f \) and smaller current density \( \frac{I_{D,m,post}}{W} \). As a matter of fact, radiation induced flicker noise increase was experimentally proven to affect in a more pronounced fashion NMOSFETs with many fingers and operated at small current densities, where the parasitic devices have a greater impact on the behavior of the main transistor [22]. On the other hand, experimental data indicate that the \( \frac{I_{D,lat,s}}{I_{D,m,post}} \) ratio is a decreasing function of the total post-irradiation drain current \( I_{D,tot} = I_{D,m,post} + 2n_f I_{D,lat,s} \), corresponding to the current forced into the device drain terminal. This is shown as an
example in Fig. 10, where the $I_{P\text{,tot}}/I_{D\text{,pre}}$ ratio is plotted as a function of $I_{D\text{,pre}}$. Upon absorption of a 10 Mrad $\gamma$-ray dose for a set of NMOSFETs with $W = 1000 \, \mu m$ and varying $L$. Equation (6) provides some hints for rad-hard front-end design, which are substantiated by the results of Fig. 11, showing the ENC normalized with respect to the pre-irradiation value averaged over several pixels in different Apsel3T1 and Apsel2T chips (the latter operated at a peaking time of 500 ns, comparable with the 400 ns peaking time of the Apsel3T1 chip). The Apsel2T MAPS are found to perform better even at larger integrated doses. This result can be explained by considering the layout features and the operating point of the preamplifier input device in the two different MAPS versions. In particular, the smaller drain current density and the larger number of fingers (see Section II) make the Apsel3T1 preamplifier input device more sensitive to ionizing radiation as far as flicker noise is concerned. These results corroborate once more the notion that, at least in the 130 nm technology node, enclosed layout transistors, with their very high degree of radiation hardness [22], are mandatory if low noise performance under irradiation is required.

C. Charge collection properties

The effects of ionizing radiation on the charge collection properties of the Apsel3T1 chips under examination have been also tested by means of an $^{55}$Fe source and a low power, infrared laser source. $^{55}$Fe sources can be used to provide charge sensitivity and noise calibration for pixels without injection capacitance and to validate measurements obtained with other methods. Fig. 12 shows the event count rate distribution for a pixel in an M2 matrix and compares pre-irradiation, post-irradiation and post-annealing spectra. A very similar behavior was found in the characterization of the other DUTs. $^{55}$Fe X-rays release their entire energy in the detector substrate through photoelectric interaction. Photons from the $^{55}$Fe 5.9 keV line generate about 1640 electron/hole pairs each. When photons convert in the junction depleted region, the released charge is virtually entirely collected, yielding the peak in the $^{55}$Fe spectrum. Charge released far from the junction and only partially collected is responsible for the pedestal at lower amplitudes. Data shown in Fig. 12 are in fair qualitative agreement with the charge sensitivity and noise results discussed in the previous sections. As the absorbed dose increases, the 5.9 keV peak gets broader as a consequence of the noise increase. At the same time, the peak is shifted towards lower amplitude values, as a result of the charge sensitivity decrease. Immediately after the first irradiation step, a non negligible loss in the count rate can be detected in the peak region. Since the count rate in the peak is proportional to the depleted substrate volume, this result might hint at a reduction in the thickness of the space charge region at the DNW-to-substrate junction. This in turn may be possibly due to a decrease in the DNW potential as a consequence of a change in the gate voltage of the preamplifier input transistor. After the annealing procedure, the $^{55}$Fe spectrum is restored almost to the original condition, only with a persisting event rate loss with respect to the pre-irradiation measurement results. Note that the charge sensitivity values provided by $^{55}$Fe measurements, between 800 and 900 mV/IC, are significantly different from the ones shown in Fig. 2. This discrepancy might be due to the actual value of the injection capacitance being sizably underestimated and considerably larger than the nominal 30 fF value. Nevertheless, once the charge sensitivity is normalized to the pre-irradiation value, $^{55}$Fe tests and charge injection through $C_{inj}$ provide fairly similar results. This is shown in Fig. 13, comparing the normalized charge sensitivities obtained, at a peaking time of 400 ns, by applying the two mentioned measurement techniques to the central pixel of the M2 matrix in chip 24.

A measurement setup for precision scanning with an infrared laser (featuring a wavelength $\lambda=1064$ nm and a beam spot of about 20 $\mu m$ in diameter) was also used to investigate the charge collection properties of the deep N-well MAPS. The samples were illuminated from the back side in order to avoid reflections from the intricate net of interconnections laid out on the front side. Note that, in this configuration,
the light, after going through the device bulk, is reflected back into the substrate by the metals at the chip top. Since the aim of the laser test is to evaluate the relative variation of the collected charge with the laser spot position inside the pixel, reflection is not expected to significantly affect the measurement results, as long as it is uniform over the cell. The latter is a reasonable assumption, as the chip top side is virtually fully covered with metal layers. Fig. 14, which is exemplary of the general behavior of the tested pixels, shows the charge collected by the central pixel of an M1 matrix as a function of the laser beam position before irradiation and after exposure to a 9700 krads SiO2 total ionizing dose. The figures also show the layout of the sensor, with a main body and three N-well satellite diffusions. The collected charge was calculated as the ratio between the amplitude of the readout channel response to the laser pulse and the charge sensitivity measured by means of charge injection through an external pulser. The matrix, which features a pitch of 50 μm in both the X and Y directions, has been scanned using a 5 μm step. The point corresponding to the maximum collected charge value was taken as the (0,0) coordinate. Before irradiation, the peak value of the collected charge is about 1000 electrons, which is close to the signal from a minimum ionizing particle (MIP). This is supported by laboratory tests performed with a 100Sr source. After irradiation a small decrease (about 5%) in the peak value of the charge collected by the DNW sensor can be noticed. This very limited effect might be ascribed to the small amount of non-ionizing energy released by 60Co γ-rays in the sensor substrate, which might be responsible for the creation of traps in the bulk (although with a very small density) through Compton scattering and, as a consequence, for an increase in the carrier recombination probability. Actually, such a small variation might also be explained with errors in the measurement setup, due to instance to slight differences in the distance between the DUT and the laser focusor from measurement to measurement. This latter hypothesis seems to find support in Fig. 15, where the peak value of the collected charge in the central pixel of M1 and M2 matrices is plotted as a function of the integrated dose and after the 100°C/168 h cycle. Although the data values at 9700 krads are 5-10% lower than the pre-irradiation values for all of the tested devices, nevertheless no clear trend with the dose can be easily determined. Also, the leakage current test results discussed in Section III seems to validate the hypothesis of a very limited, if not completely absent, bulk damage.

IV. CONCLUSION

In this paper, results from total ionizing dose characterization of deep N-well monolithic sensors fabricated in a 130 nm CMOS technology have been presented and discussed. A large set of devices have been irradiated with γ-ray doses up to about 10 Mrad(SiO2) (a relatively high integrated dose as far as MAPS are concerned) in view of applications to the vertex detector for the SuperB Factory experiment. DUTs were also subjected to a 100°C/168 h cycle. At the highest integrated dose, a decrease of 20-30% in the charge sensitivity and an
increase well in excess of 100% in the equivalent noise charge have been detected. Increase in the sensor leakage current was proved to result mainly from hole buildup in the field oxide over the junction and/or trap creation at the SiO₂/Si interface. The analysis of charge collection properties of irradiated DNW MAPS, carried out by means of an ⁶⁰Fe and an infrared laser source, did not indicate any major performance degradation. The results presented in this work gather new evidence to support the damage mechanisms proposed in a previous radiation tolerance study on a very similar structure irradiated at much lower doses. They also provide a set of useful rules for hard design of DNW MAPS and, more generally, of analog front-end in deep submicron CMOS processes. Irradiation with a monochromatic neutron source is being planned to study MAPS sensitivity to bulk damage. Moreover, new Apsel samples will be irradiated with a low dose rate γ-ray source and subjected to room (or under 100°C) temperature annealing cycles to investigate their behavior under conditions closer to the real application.

ACKNOWLEDGMENT

The authors wish to thank A. Faucitano (Università di Pavia), who made the ⁶⁰Co source available for device irradiation, and M. Dellagiovanua, who carried out a large part of the measurements presented in this work. They are also indebted to V. Speziali (Università di Pavia) for her useful suggestions.

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